Department of Electronics and Communication Engineering

M.Tech. Internet of Things
Curriculum and Syllabus

(Applicable to the students admitted from AY: 2023 onwards)

School of Engineering and Sciences
SRM University *AP*, Andhra Pradesh

Department Vision

To be a globally recognized leader in the field of Electronics and Communications, by fostering innovation through cutting-edge collaborative research to deliver a world-class interdisciplinary education.

Department Mission

1. Create inclusive and highly motivated individuals and leaders who promote diversity, innovation, creativity, and a high sense of responsibility towards societal progress.
2. Strive for excellence by promoting interdisciplinary education and research through global collaborations.
3. Deliver state-of-the-art research-based education that equips students with the skills to address contemporary challenges and contribute to the field's advancement.
4. Foster a culture of innovation and entrepreneurship, by working closely with leading industry partners to translate ideas into real-life solutions.
5. Aim to be a global knowledge hub by collaborating with leading institutions and industries.

Program Educational Objectives (PEO)

1. Enable the postgraduate students to be proficient in Embedded Systems and Internet of Things and develop strong skills and competencies for their professional careers and higher studies.
2. Gain hands-on learning experiences in Embedded System Design skills which can be applied to find exceptional solutions to industrial and research problems in an inter-disciplinary environment.
3. Develop effective communication skills, lifelong learning, leadership qualities and ethical professional conduct across their higher education and career paths.

Mission of the Department to Program Educational Objectives (PEO) Mapping

	PEO 1	PEO 2	PEO 3
Mission Statement 1	3	1	2
Mission Statement 2	3	3	2
Mission Statement 3	2	1	3
Mission Statement 4	3	2	3
Mission Statement 5	3	3	2

Program Specific Outcomes (PSO)

1. Design and integrate embedded systems solutions for real-life and industrial scenarios using appropriate technology and tools.
2. Develop secure and scalable Internet of Things for efficient communication.
3. Conduct exceptional research in the field of Embedded Systems and the Internet of Things using advanced technologies & platforms, analyse data and report.

Mapping Program Educational Objectives (PEO) to Program Learning Outcomes (PLO)

Program Learning Outcomes (PLO)													
PEOs	POs										PSOs		
	Engineering Knowledge	Design Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Lifelong Learning	PSO 1	PSO 2	PSO 3
PEO 1	3	3	3	3	2	1	3	2	2	2	3	2	2
PEO 2	3	3	3	3	3	1	3	1	2	2	3	2	3
PEO 3	3	3	3	3	2	3	3	3	3	3	2	3	3

Category Wise Credit Distribution			
Course Sub-Category	**Sub-Category Credits**	**Category Credits**	**Learning Hours**
Ability Enhancement Courses (AEC)		1	30
University AEC	0		
School AEC	1		
Value Added Courses (VAC)		1	30
University VAC	0		
School VAC	1		
Skill Enhancement Courses (SEC)		4	120
School SEC	4		
Department SEC	0		
SEC Elective	0		
Foundation / Interdisciplinary courses (FIC)		3	90
School FIC	0		
Department FIC	3		
Core + Core Elective including Specialization (CC)		36	1080
Core	28		
Core Elective (Inc Specialization)	8		
Minor (MC) + Open Elective (OE)	0	0	0
Research / Design / Internship/ Project (RDIP)		35	1050
Internship / Design Project / Startup / NGO	3		
Internship / Research / Thesis	32		
Total		**80**	**2400**

Semester wise Course Credit Distribution Under Various Categories						
Category	**Semester**					
	I	**II**	**III**	**IV**	**Total**	**%**
Ability Enhancement Courses - AEC	1	1	0	0	2	2
Value Added Courses - VAC	0	1	0	0	1	1
Skill Enhancement Courses - SEC	2	2	0	0	4	5
Foundation / Interdisciplinary Courses - FIC	3	0	0	0	3	4
CC / SE / CE / TE / DE / HSS	16	20	0	0	36	44
Minor / Open Elective - OE	0	0	0	0	0	0
(Research/ Design/ Industrial Practice/Project/Thesis/Internship) - RDIP	0	3	17	15	35	43
Grand Total	**22**	**27**	**17**	**15**	**81**	**100**

Note: L-T/D-P/Pr and the class allocation is as follows.

a) Learning Hours : 30 learning hours are equal to 1 credit.

b) Lecture/Tutorial : 15 contact hours (60 minutes each) per semester are equal to 1 credit.

c) Discussion : 30 contact hours (60 minutes each) per semester are equal to 1 credit.

d) Practical : 30 contact hours (60 minutes each) per semester are equal to 1 credit.

e) Project : 30 project hours (60 minutes each) per semester are equal to 1 credit.

SEMESTER - I								
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**
1	VAC	U VAC	VAC 501	Community Engagement and Social Responsibility	0	0	1	1*
2	SEC	S SEC	SEC 502	Design Thinking	1	0	1	2
3	FIC	D FIC	FIC 503	AI/ML Techniques	2	0	1	3
4	Core	CC	EIT 501	Embedded Programming	3	0	1	4
5	Core	CC	EIT 502	Embedded Networking	3	0	1	4
6	Core	CC	EIT 503	Smart Sensors and Actuators	3	0	1	4
7	Core	CC	EIT 504	Computer Network and Internet Protocol	3	0	1	4
8	AEC	AEC	AEC 502	Research Seminar - I	0	0	1	1
				Semester Total	**15**	**0**	**8**	**22**

SEMESTER - II								
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**
1	VAC	U VAC	VAC 502	Community Engagement and Social Responsibility	0	0	1	1
2	SEC	SEC	SEC 103	Entrepreneurial Mindset	1	0	1	2
3	Core	CC	IOT 505	IoT Architecture and Protocols	3	0	1	4
4	Core	CC	IOT 506	SOC Design for IoT	3	0	1	4
5	Core	CC	IOT 507	Wireless Sensor Networks & IoT	3	0	1	4
6	Elective	CE	CE	Industry - Core Elective				4
7	Elective	CE	CE	Industry - Core Elective				4
8	RDIP	RDIP	IOT 508	Project Management	0	0	3	3
9	AEC	AEC	AEC 503	Research Seminar - II	0	0	1	1
				Semester Total	**0**	**2**	**2**	**27**

SEMESTER - III								
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**
1	RDIP	RDIP	IOT 509	Thesis - I	0	0	14	14
2	RDIP	RDIP	IOT 510	Industrial Practice	0	0	3	3
				Semester Total	**0**	**0**	**17**	**17**

SEMESTER - IV								
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**
1	RDIP	RDIP	IOT 511	Thesis - II	0	0	15	15
				Semester Total	**0**	**0**	**15**	**15**

List of Core Electives								
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**
1	CE	CE	IOT 532	Designing Embedded systems with UML	3	1	0	4
2	CE	CE	IOT 543	Hardware Security for IoT	3	1	0	4
3	CE	CE	IOT 558	Deep Learning for IoT	3	0	1	4
4	CE	CE	IOT 531	Hardware Accelerators for IoT edge computing	3	0	1	4
5	CE	CE	IOT 530	FPGA Design for Embedded systems	3	0	1	4

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Design Thinking

Course Code	SEC 502	Course Category	SEC	L	T	P	C
				1	0	1	2
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)			
Course Offering Department	Management	Professional / Licensing Standards					

Course Objectives / Course Learning Rationales (CLRs)

1. Familiarize with the principles of Design Thinking
2. Learn to apply the principles of Design Thinking
3. Apply Design Thinking to solve problems.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Grasp the Concepts and process of Design Thinking	1	85%	90%
Outcome 2	Learn the process of Design Thinking	1	85%	90%
Outcome 3	Solve a problem using Design Thinking Principles	3	75%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

PEOs	Program Learning Outcomes (PLO)												
	POs										PSOs		
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tool Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork	Communication	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3									1	3	1	3
Outcome 2	3							3		2	3	2	3
Outcome 3	3	3	3	3				3	3	3	3	3	3
Average	3	3	3	3				3	3	2	3	2	3

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Incubation and understanding**			1,2
	Understanding of Design Thinking & its Importance	4	1	1,2
	Importance of Design Thinking	3	1	1,2
	Pillars of Design Thinking	3	1	1,2
Unit 2	**Process – Understanding the Stages of Design Thinking**			1,2
	Stage 1- Empathy	2	2	1,2
	Stage 2 - Define	2		
	Stage 3 – Ideate	2		
	Stage 4 – Prototype	2	2	1,2
	Stage 5 – Test & Implement	2	2	1,2
Unit 3	**Application**			
	Project Work	7	3	1,2
	Viva	3	3	1,2
Total Contact Hours		**30**		

Learning Assessment

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (100%)**	
		CLA-1 (50%)	**CLA-2 (50%)**
Level 1	Remember	20	40
	Understand		
Level 2	Apply	30	30
	Analyse		
Level 3	Evaluate	50	30
	Create		
Total		**100%**	**100%**

Recommended Resources

1. Design Thinking – Techniques and Approaches, N. Siva Prasad

Other Resources

1. HBS – Online – Design Thinking & Innovation – course material
2. Case studies
3. Nigel Cross , Design Thinking, BERG Publishing, (2011)
4. Thomas Lockwood , Design Thinking- Integrating Innovation, Customer Experience and Brand Value, , Design Management Institute, (2009)

Course Designers

1. Satyanarayana Duvvuri, Visiting Faculty, Paari school of business, SRM University AP.

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Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

AI/ML Techniques

Course Code	FIC 503	**Course Category**	FIC	**L**	**T**	**P**	**C**
				2	0	1	3
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To familiarise the domains of supervised and unsupervised learning.
2. To understand and apply various binary classifiers.
3. To understand and apply clustering methods.
4. To understand and analyse Feedforward neural networks and CNNs
5. Able to work on real time projects related to AI/ML

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Familiarise supervised and unsupervised learning	1	85%	80%
Outcome 2	Understand and Apply various binary classifiers	1, 2	80%	75%
Outcome 3	Understand and Apply clustering methods	1, 2	85%	70%
Outcome 4	Understand and Apply Feedforward neural networks	2	80%	70%
Outcome 5	Understand the CNNs and able to work on real time projects	1,2	75%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	1	1	1	1						1	1	1	1
Outcome 2	2	2	3	2				2	1	1	1	2	3
Outcome 3	2	2	2	3				2	1	1	1	2	2
Outcome 4	2	3	3	3				2	1	1	2	3	3
Outcome 5	3	2	3	3				2	1	2	2	2	2
Average	2	2	3	3				2	1	1	1	2	2

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Introduction**	**6**		
1.	Introduction to machine learning	1	1	1, 2,3
2.	Supervised learning	1	1	1, 2,3
3.	Unsupervised learning	1	1	1, 2,3
4.	Linear regression	1	1	1, 2,3
5.	Logistic regression	2	1	1, 2,3
Unit 2	**Classifiers**	**5**		
6.	Naive Bayes	1	2	1, 2,3
7.	Support Vector Machines	1	2	1, 2,3
8.	K-Nearest Neighbor	1	2	1, 2,3
9.	Decision Trees	1	2	1, 2,3
10.	Random forest	1	2	1, 2,3
Unit 3	**Clustering**	**6**		
11.	Clustering in machine learning	1	3	1, 2,3
12.	Different types of clustering algorithms	1	3	1, 2,3
13.	K-Means clustering	1	3	1, 2,3
14.	Loss functions in regression and classification	2	3	1, 2,3
15.	Bias-variance trade off	1	3	1, 2,3
Unit 4	**Feedforward neural networks**	**7**		
16.	Introduction to Neural Networks	1	4	1, 2,3
17.	Activation functions	1	4	1,2,3
18.	Feed-forward Network	1	4	1, 2,3
19.	Backpropagation algorithm	2	4	1, 2,3
20.	Introduction to convolutional neural network (CNN)	2	5	1, 2,3
Unit 5	**Applications of AI/ML**	**6**		
21.	Applications in VLSI	3	5	4
22.	Applications in IoT	3	5	4
Total Contact Hours		**30**		

Course Unitization Plan – Lab

Session	Description of Experiment	Contact hours required	CLOs Addressed	Reference Used
1	Implement Linear Regression on the given dataset using Python/MATLAB	2	1	1, 2,3
2	Implement Naïve Bayes classifier using Python/MATLAB	2	1	1, 2,3
3	Implement Logistic Regression on the given dataset using Python/MATLAB	2	1	1, 2,3
4	Implement SVM algorithm using Python/MATLAB	2	2	1, 2,3
5	Implement Decision Tree classifier using Python/MATLAB	2	2	1, 2,3
6	Implement Random Forest classifier using Python/MATLAB	2	2	1, 2,3
7	Implement K-means algorithm for clustering the data using python/MATLAB	2	3	1, 2,3
8	Implement K-Nearest Neighbor classifier using python/MATLAB	2	2	1, 2,3
9	Emulate logic gates using neural Network using python	2	4	1, 2,3
10	Implement single-Layer Neural Network for image/data analysis using Python/MATLAB	4	4	1, 2,3
11	Implement Convolution Neural Network for image/data analysis using Python/MATLAB	4	5	1, 2,3
12	Implement Markov model for analysis of stock market data using python/MATLAB	4	1	1, 2,3
Total Contact Hours		**30**		

Learning Assessment- Theory

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)								End Semester Exam (50%)	
		CLA-1 (10%)		Mid-1 (15%)		CLA-2 (10%)		CLA-3 (15%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	40%	40%	60%	40%	40%	40%	60%	40%	30%	40%
	Understand										
Level 2	Apply	60%	60%	40%	60%	60%	60%	40%	60%	70%	60%
	Analyse										
Level 3	Evaluate										
	Create										
Total		**100%**		**100%**		**100%**		**100%**		**100%**	

Learning Assessment – Lab

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		Experiments (15%)	Record / Observation Note (10%)	Viva + Model (25%)	
Level 1	Remember	30%	70%	30%	30%
	Understand				
Level 2	Apply	70%	30%	70%	70%
	Analyse				
Level 3	Evaluate				
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Christopher M. Bishop, "Pattern Recognition and Machine Learning" by Springer, 2007.
2. Tom M. Mitchell, "Machine Learning", First Edition by Tata McGraw-Hill Education, 2013.
3. Luis G. Serrano, "Grooking Machine Learning" 2nd Edition, Manning Publications, 2021.
4. Reference papers from various journals such as IEEE, Elsevier etc.

Other Resources

Course Designers

1. Dr. Sudhakar Tummala. Asst. Professor, Dept. Of ECE. SRM University - AP
2. Dr. V. Udaya Sankar, Asst. Professsor, Dept. Of ECE. SRM University - AP

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Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Embedded Programming

Course Code	EIT 501	**Course Category**	CC	**L**	**T**	**P**	**C**
				3	0	1	4
Pre-Requisite Course(s)	Microprocessors and Microcontrollers	**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	Electronics and Communication Engineering	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. Understand the basics of Embedded Systems.
2. Learn the ARM architecture, instruction set and its assembly programming.
3. Learn to develop C programs for ARM processors and interfacing the peripherals.
4. Understand the software architectures used in Embedded Systems.
5. Learn the embedded system security including the network security

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand and explain the basics of Embedded Systems.	1	80%	70%
Outcome 2	Understand the ARM Cortex M Architecture, instruction set and do ARM assembly & C programming.	2	80%	70%
Outcome 3	Understand the architecture used in Embedded Software	1	80%	70%
Outcome 4	Understand the RTOS concepts and develop RTOS applications for ARM Microcontrollers.	2	80%	70%
Outcome 5	Understand various Embedded System Attacks & its security measures.	1	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2	1				1		1	1	1	1
Outcome 2	3	3	3	1				1		2	2	2	2
Outcome 3	3	1	2	1				1		1	2	2	2
Outcome 4	3	1	3	1				1		2	2	2	2
Outcome 5	3	1	2	1				1		2	2	2	2
Average	3	1	2	1				1		2	2	2	2

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**OVERVIEW**	**9**		
1	Embedded System Case Studies	2	1	1,3
2	Introduction to Embedded Systems	2	1	1,3,4
3	Getting to Know the Hardware	2	1	1,3,4
4	Learn How to Communicate	1	1	1,3,4
5	Getting to Know the Processor	1	1	1,3,4
6	Study the External Peripherals	1	1	1,3,4
Unit 2	**ARM REFERENCE ARCHITECTURE**	**9**		
7	ARM Processor Architecture	1	**2**	1,3,4
8	ARM Software Development	1	2	1,3,4
9	ARM Instruction Sets	1	2	1,3,4
10	Getting Started with Embedded Software Development (Tools, Packages, Platforms, etc.)	1	2	1,3,4
11	Your First Embedded Program-Hello, ARM!	1	2	1,3,4
12	The Blinking LED Program	1	2	1,3,4
13	The Role of the Infinite Loop	1	2	1,3,4
14	Compiling, Linking, and Locating	1	2	1,3,4
15	The Build Process	1	2	1,3,4
Unit 3	**SOFTWARE ARCHITECTURE**	**11**		
18	Four types of common architectures	3	3	3
19	Peripherals (drivers)	2	3	3
20	Interrupts (ISR, IVT, pitfalls, etc.)	1	3	3,5
21	Round-Robin	2	3	3,5
22	The Shared Data Problems	2	3	3,5
23	Function-Queue-Scheduling Architecture	1	3	3
Unit 4	**EMBEDDED OPERATING SYSTEM**	**10**		
27	Real-Time Operating Systems	3	4	2,8
28	Interrupt Routines in an RTOS Environment	2	4	2,8
29	Tasks and Task States	3	4	2,8
30	Tasks and Data	2	4	2,8
Unit 5	**EMBEDDED PROGRAMMING AND SECURITY**	**6**		
31	Embedded Systems Attacks: Uniquely Embedded Insecurities	3	5	2
32	Attackers and Assets: Common Firmware Vulnerabilities	2	5	2
33	Java: Concurrency, Pitfalls, and Wireless Applications	1	5	2
	Total Contact Hours	**45**		

Course Unitization Plan – Lab

Session	Description of Experiment	Contact hours required	CLOs Addressed	Reference Used
1.	ARM Assembly language program for doing arithmetic operation.	2	2	6,8
2.	ARM assembly language program for Memory operations	2	2	6,8
3.	ARM Assembly - Interfacing memory mapped peripherals 1. Binary Counter with LEDs 2. Real Time Clock 3. Analog to Digital converter 4. Digital to Analog Converter	4	2	6
4.	C Program for peripheral interfacing 1. GPIO 2. Real Time Clock 3. Analog to Digital Converter 4. Digital to Analog Converter	4	2	6
5.	C Program for Asynchronous and synchronous serial communication 1. UART 2. I2C/SPI	4	2	6
6.	Embedded Ethernet applications	4	2	6
7.	Controller Area Network (CAN) interface	2	2	6
8.	RTOS Task Management	2	3	8
9.	RTOS Inter Task Synchronization and Inter Task communication	4	3	8
10.	Mini Capstone Project	2	2,3	
Total Contact Hours		**30**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)								End Semester Exam (50%)	
		CLA-1 (15%)		Mid-1 (15%)		CLA-2 (10%)		CLA-III (10%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	40%		30%		40%		40%		50%	
	Understand										
Level 2	Apply	60%		70%		60%		60%		50%	
	Analyse										
Level 3	Evaluate										
	Create										
Total		**100%**		**100%**		**100%**		**100%**		**100%**	

Learning Assessment – Lab

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		Experiments (15%)	Record / Observation Note (10%)	Viva + Model (25%)	
Level 1	Remember	30%	70%	30%	30%
	Understand				
Level 2	Apply	70%	30%	70%	70%
	Analyse				
Level 3	Evaluate				
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Barr, Michael, and Anthony Massa. Programming embedded systems: with C and GNU development tools. " O'Reilly Media, Inc.", 2006.
2. Simon, David E. An embedded software primer. Vol. 1. Addison-Wesley Professional, 1999.
3. Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, MIT Press, ISBN 978-0-262-53381-2, 2017.
4. Richard Barnett, Sarah Cox, Larry O'Cull, Embedded C programming and the Atmel AVR. 2 edition. Clifton Park, N.Y. : Thomson Delmar Learning (532 p).
5. Wolf, Wayne (2008), Computers as components : principles of embedded computing system design. 2 edition. Amsterdam : Elsevier (507 p).
6. Ata Elahi, Trevor Arjeski, “ARM Assembly Language with Hardware Experiments”, Springer, 2015.
7. A.N.Sloss et al., “ARM System Developer’s Guide”, Morgan Kaufmann Publishers, 2004

Other Resources

Course Designers

1. Dr Ramakrishnan M. Associate Professor, Department of Electronics and Communication Engineering, SRM University - AP

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Embedded Networking

Course Code	EIT 502	**Course Category**	CC	**L**	**T**	**P**	**C**
				3	0	1	4
Pre-Requisite Course(s)	Microprocessors and Microcontrollers	**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	Electronics and Communication Engineering	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. Application Development using USB and CAN bus with microcontrollers.
2. Understand the lightweight TCP/IP protocol and its usage.
3. Understand the MODBUS RTU and MODBUS TCP protocols.
4. Application development for 6LoWPAN network on Contiki OS.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand Embedded Communication Protocols like UART, RS232, RS485, SPI, I2C.	1	80%	70%
Outcome 2	Understand and apply the Controller Area Network and Local Interconnect Network	2	80%	70%
Outcome 3	Develop Embedded TCP/IP applications.	2	80%	70%
Outcome 4	Understand and develop application using Modbus RTU and Modbus TCP	2	80%	70%
Outcome 5	Develop simple Contiki applications and simulate it using COOJA simulator.	2	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2				1	1	1	1	1	3	2
Outcome 2	3	3	3				1	1	2	2	2	3	3
Outcome 3	3	3	3				1	1	2	2	2	3	3
Outcome 4	3	3	3				1	1	2	2	2	3	3
Outcome 5	3	1	2				1	1	2	2	2	3	2
Average	**3**	**2**	**2**				**1**	**1**	**2**	**2**	**2**	**3**	**2**

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**EMBEDDED COMMUNICATION PROTOCOLS**	**9**		
1.	Embedded Networking - Introduction	1	1	1,3
2.	Serial/Parallel Communication	1	1	1,3
3.	Serial communication protocols - RS232 standard – RS485	1	1	1,3
4.	Synchronous Serial Protocols -Serial Peripheral Interface (SPI)	1	1	1,3
5.	Inter Integrated Circuits (I2C)	1	1	1,3
6.	PC Parallel port programming	1	1	2
7.	ISA/PCI Bus protocols	1	1	1,3
8.	Firewire	1	1	1,3
Unit 2	**USB, CAN AND LIN BUS**	**8**		
9.	USB bus – Introduction	1	1	1,3
10.	Speed Identification on the bus, USB States	1	1	3
11.	USB bus communication: Packets –Data flow types, Enumeration –Descriptors	1	1	3
12.	USB Device Classes (CDC, MSC, HID) and USB Host	1	1	3
13.	CAN Bus – Introduction	1	2	3
14.	Frames –Bit stuffing –Types of errors –Nominal Bit Timing	1	2	3
15.	A simple application with CAN	1	2	3
16.	Local Interconnect Network (LIN)	2	2	4
Unit 3	**EMBEDDED TCP/IP**	**9**		
17.	Light Weight TCP/IP - Introduction	1	3	7
18.	Process model, Memory management and Network Interfaces	2	3	7,8
19.	IP Processing	2	3	7,8
20.	UDP, TCP Processing	2	3	7,8
21.	Interfacing the stack – API	1	3	7,8
22.	TCP/UDP Server Client	1	3	7,8
23.	HTTP Server, SSI and CGI	1	3	7,8
Unit 4	**MODBUS**	**9**		
25.	Modbus RTU - Introduction	1	4	5
26.	Protocol Description – Data Encoding – Data Model – Address Model	1	4	5
27.	MODBUS Transaction – Function code categories	1	4	5
28.	Function code descriptions	2	4	5
29.	Modbus Exception Responses	1	4	5
30.	Modbus TCP/IP – Protocol Description	1	4	5,6
31.	TCP Connection Management	2	4	5.6
Unit 5	**CONTIKI OS & 6LOWPAN**	**10**		
32.	Contiki OS -Introduction	1	5	9
33.	Hello World Program – Cooja Simulator	1	5	9
34.	Basic Programming	1	5	9
35.	Concurrency	2	5	9
36.	Networking in Contiki	1	5	9
37.	UDP Network Simulation	1	5	9
38.	IPV6 Networking	1	5	9
39.	Routing on Contiki -IPV6 Multicast	1	5	9
40.	6LowPAN implementation with COOJA	1	5	9
	Total Contact Hours	**45**		

Course Unitization Plan – Lab

Session	Description of Experiment	Contact hours required	CLOs Addressed	Reference Used
1	I2C/SPI Communication	2	1	9,10
2	RS485 Bus Communication – Modbus RTU	4	1,4	9,10
3	Embedded TCP/UDP application	4	3	9
4	Modbus TCP	2	4	9
5	Embedded HTTP	2	3	9
6	USB -CDC Class, HID Class	4	1	9
7	CAN/LIN communication	2	2	9
8	Contiki OS- Hello World	2	5	11
9	UDP Network simulation - Cooja	4	5	11
10	6LOWPAN simulation - Cooja	4	5	11
Total Contact Hours		**30**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)								End Semester Exam (50%)	
		CLA-1 (15%)		Mid-1 (15%)		CLA-2 (10%)		CLA-III (10%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	40%		30%		40%		40%		50%	
	Understand										
Level 2	Apply	60%		70%		60%		60%		50%	
	Analyse										
Level 3	Evaluate										
	Create										
Total		**100%**		**100%**		**100%**		**100%**		**100%**	

Learning Assessment – Lab

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		Experiments (15%)	Record / Observation Note (10%)	Viva + Model (25%)	
Level 1	Remember	30%	70%	30%	30%
	Understand				
Level 2	Apply	70%	30%	70%	70%
	Analyse				
Level 3	Evaluate				
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Frank Vahid, Givargis 'Embedded Systems Design: A Unified Hardware/Software Introduction', Student Edition, Wiley Publications, 2006.
2. Jan Axelson, 'Parallel Port Complete: Programming, Interfacing, & Using the PC's Parallel Printer', First Edition, Penram publications, 1997.
3. Microchip Technology, "AN2059 LIN Basics and Implementation of the MCC LIN Stack Library
4. on 8-Bit PIC® Microcontrollers", http://ww1.microchip.com/downloads/en/appnotes/00002059b.pdf.
5. Modbus.org, "MODBUS APPLICATION PROTOCOL SPECIFICATION V1.1b3", https://www.modbus.org/docs/Modbus_Application_Protocol_V1_1b3.pdf
6. Modbus.org, "MODBUS MESSAGING ON TCP/IP IMPLEMENTATION GUIDE V1.0b", https://www.modbus.org/docs/Modbus_Messaging_Implementation_Guide_V1_0b.pdf
7. Adam Dunkels, "Design and Implementation of the lwIP", https://www.artila.com/download/RIO/RIO-2010PG/lwip.pdf
8. Microchip Technology, Microchip TCP/IP Lite Stack, https://ww1.microchip.com/downloads/en/Appnotes/Microchip-AN1921-8-bit-PICMCU-TCP-IP-LiteStack-ApplicationNote-00001921D.pdf2
9. Agus Kurniawan, "Practical Contiki-NG, Programming for Wireless Sensor Networks", Apress, 2018
10. Dogan Ibrahim, 'Advanced PIC microcontroller projects in C', Elsevier 2008
11. Edward Insam, "TCP/IP Embedded Internet Applications", Newnes, 2003
12. Agus Kurniawan, "Practical Contiki-NG, Programming for Wireless Sensor Networks", Apress, 2018

Other Resources

Course Designers

1. Dr Ramakrishnan M. Associate Professor, Department of Electronics and Communication Engineering, SRM University – AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Smart Sensors and Actuators

Course Code	EIT 503	**Course Category**	CC		**L**	**T**	**P**	**C**
					3	0	1	4
Pre-Requisite Course(s)	Electrical & Electronic Measurement, Control Systems, Embedded System.	**Co-Requisite Course(s)**		**Progressive Course(s)**				
Course Offering Department	ECE	**Professional / Licensing Standards**						

Course Objectives / Course Learning Rationales (CLRs)

1. To understand the basics and standards of Smart sensors.
2. To study different types of Sensors.
3. To study different types of Actuators.
4. To use smart sensors in the control system applications.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the basics and manufacturing of sensors	1	90%	80%
Outcome 2	Design and applications of strain, force, torque, and pressure sensors	2	80%	80%
Outcome 3	Design and applications of motion and level sensors	2	70%	75%
Outcome 4	Understand the functioning and application of actuators	1	60%	75%
Outcome 5	Designing a control system with smart sensors and applications	2	80%	80%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	-	2	2			1	3	1	3	2	1	
Outcome 2	3	2	2	2			1	3	1	3	3	2	
Outcome 3	3	2	2	2			1	3	1	3	3	2	
Outcome 4	3	-	2	2			1	3	1	3	3	2	
Outcome 5	3	-	2	2			1	3	1	3	3	3	3
Average	3	2	2	2			1	3	1	3	3	2	3

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Fundamental of Smart Sensors**	**10**		
1.	Basics of smart sensors	1	1	1
2.	general sensing system, definition of smart sensor, Smart sensor model,	1	1	1,5
3.	Micromachining	2	1	1
4.	parameters, characteristics, environmental parameters, Performance, error Analysis characteristics.	1	1	1,2
5.	Excitation, Amplification, Filters, Converters, Compensation, Information Coding/Processing, Data Communication	2	1	1,2
6.	Sensor Communication and MEMS	1	1	1,2
7.	Standards for smart sensors	2	1	1
Unit 2	**Strain, Force, Torque and Pressure sensors**	**6**		
8.	Strain gages, strain gage beam force sensor,	1	2	2,4
9.	piezoelectric force sensor, load cell, torque sensor,	1	2	2,4
10.	Piezo-resistive and capacitive pressure sensor,	1	2	2,4
11.	optoelectronic pressure sensors, vacuum sensors	1	2	2,4
12.	Design of signal conditioning circuits for strain gauges, piezo, capacitance and optoelectronics sensors	2	2	2,4
Unit 3	**Motion and Level Sensors**	**13**		
13.	Potentiometric and capacitive sensors, Inductive and magnetic sensor,	1	3	2,4
	LVDT, RVDT, eddy current, transverse inductive,	2	3	2,4
14.	Hall effect, magneto resistive, magneto strictive sensors	2	3	2,4
15.	Fiber optic liquid level sensing, Fabry Perot sensor,	1	3	2,4
16.	ultrasonic sensor, capacitive liquid level sensor.	1	3	2,4
17.	Signal condition circuits for reactive and self-generating sensors.	1	3	2,4
18.	Electromagnetic velocity sensor, Doppler with sound, light,	2	3	2,4
19.	Accelerometer characteristics, capacitive, piezo-resistive, piezoelectric accelerometer, thermal accelerometer,	2	3	2,4
20.	rotor, monolithic and optical gyroscopes.	1	3	2,4
Unit 4	**Actuators**	**10**		
21.	Actuation systems, Pneumatic and hydraulic systems, Directional Control valves, Pressure control valves,	2	4	3
22.	Cylinders, Servo and proportional control valves, Process control valves,	1	4	3
23.	Rotary actuators, Mechanical Actuation Systems, Types of motion, Kinematic chains,	2	4	3
24.	Cams, Gears, Ratchet and pawl, Belt and chain drives, Bearings,	1	4	3
25.	Mechanical aspects of motor selection, Electrical Actuation Systems,	1	4	3
26.	Electrical systems, Mechanical switches, Solid-state switches, Solenoids,	2	4	3
27.	D.C. Motors, A.C. Motors, Stepper motors.	1	4	3
Unit 5	**Sensors in a Control Loop**	**6**		
	Programmable logic controllers, Open- Vs Closed-loop systems,	1	5	1
28.	PID control	1	5	1
29.	Fuzzy logic and neural networks	2	5	1
30.	Adaptive control	1	5	1
31.	Impact of AI on sensing	1	5	1
Total Contact Hours		**45**		

Course Unitization Plan – Lab

Exp No.	Experiment Name	Required Contact Hours	CLOs Addressed	References Used
	Demonstration of Arduino Kit and other hardware peripherals.	4 Hours	-	6,7,8
	Demonstration of Virtual Lab.	3 Hours	-	9
1.	Study the characteristics of temperature sensor (RTD).	3 Hours	2	6,7,8
2.	Study the characteristics of DHT11 using Raspberry Pi.	2 Hours	2	6,7,8
3.	Demonstration of image capturing using IR camera with Raspberry Pi.	3 Hours	2	6,7,8
4.	Study the characteristics of Strain gauge.	3 Hours	2	6,7,8
5.	Study the characteristics of DC Motor using Arduino IDE.	2 Hours	3	6,7,8
6.	Study the characteristics of Servo Motor using Arduino IDE.	2 Hours	3	6,7,8
7.	Study the characteristics of Stepper Motor using Arduino IDE.	2 Hours	3	6,7,8
8.	Study the characteristics of Light sensor.	2 Hours	2	6,7,8
9.	Study the characteristics of Microphone sensor.	2 Hours	2	6,7,8
10.	Study the characteristics of Air pressure sensor	2 Hours	3	6,7,8
Total Contact Hours		**30 hours**		

Learning Assessment (Theory)

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (40%)**				**End Semester Exam (20%)**
		Theory (40%)				
		Mid – 1 (15%)	**CLA -1 (5%)**	**CLA-2 (10%)**	**CLA-3 (10%)**	**Theory (40%)**
Level 1	Remember	55%	45%	40%	40%	37%
	Understand					
Level 2	Apply	45%	55%	60%	60%	63%
	Analyse					
Level 3	Evaluate					
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Learning Assessment (Lab)

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (30%)**			**End Semester Exam (10%)**
		Lab Performance (15%)	**Model Exam (10%)**	**Observation Note (5%)**	
Level 1	Remember	30%	30%	70 %	30%
	Understand				
Level 2	Apply	70%	70%	30%	70%
	Analyse				
Level 3	Evaluate				
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Randy Frank," Understanding Smart Sensors", Artech House Publication, 2013, Edition 3.
2. D. Patranabis, "Sensors and Transducers", PHI Learning Private Limited, Edition 2.
3. W. Bolton, "Mechatronics", Pearson Education Limited.
4. Jacob Fraden, "Hand Book of Modern Sensors: physics, Designs and Applications", 2015, 3rd edition, Springer, New York.
5. Jon. S. Wilson, "Sensor Technology Hand Book", 2011, 1st edition.
6. Agus Kurniawan, "Internet of Things Projects with ESP32", Packt Press, 2019.
7. Neil Cameron, "Electronics Projects with the ESP8266 and ESP32", APress, 2020.
8. https://m5stack.oss-cn-shenzhen.aliyuncs.com/resource/docs/Demo-Board_en_sht30.pdf
9. https://www.vlab.co.in/

Other Resources

Course Designers

1. Dr. Arijit Datta, Assistant Professor, Dept. of ECE. SRM University – AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Computer Networks and Internet Protocol

Course Code	EIT 504	Course Category	CC	L	T	P	C
				3	0	1	4
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)			
Course Offering Department	ECE	Professional / Licensing Standards					

Course Objectives / Course Learning Rationales (CLRs)

1. To Understand the computer network.
2. To Understand internet and protocols.
3. To Study how to apply internet protocols on IOT.
4. Understand the importance of protocols.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Describe the basics and structures of Computer network	1	75%	70%
Outcome 2	Identifies the different types of network layers	1	75%	70%
Outcome 3	Identifies different protocols in the different layers	1	75%	70%
Outcome 4	Understand and build the skills on wireless technologies and Internet of things	2	75%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	1	1								2	2	1	
Outcome 2	2	1							1	2	2	2	
Outcome 3	1	2	2						1	3	3	1	2
Outcome 4	1	2	2						1	3	3	1	2
Average	2	2	2						1	3	3	2	2

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit I	**Introduction**	**9**		
1.	Introduction to Computer Networks	2	1	1,2
2.	Data network	2	1	1,2
3.	Circuit Switching Network	2	2	1,2
4.	Packet Switching Network	2	1	1,2
5.	TCP/IP Protocol Stack	1	2	1,2
Unit II	**Application Layer**	**8**		1,2
6.	Introduction to application layer	2	2	1,2
7.	Introduction to HTTP, FTP	2	3	1,2
8.	Email, DNS	2	3	1,2
9.	World wide web	2	3	1,2
Unit III	**Transport Layer**	**9**		
10.	Introduction to Transport Layer Connection Establishment and Closure	2	3	1,2
11.	Flow Control at the Transport Layer	2	3	1,2
12.	Congestion Control	2	3	1,2
13.	Transmission Control Protocol – Basic Features, TCP Congestion Control	3	3	1,2
Unit IV	**Recognition And Reconstruction**	**9**		
14.	Introduction to Transport layer	2	2	1,2
15.	Intra Domain Routing Protocols	2	3	1,2
16.	Inter Domain Routing Protocols (BGP)	2	3	1,2
17.	Simple Network Management Protocol (SNMP)	3	3	1,2
Unit V	**Wireless LAN**	**10**		
18.	Introduction to IOT	3	4	1,2
19.	Network security	3	4	1,2
20.	WiMAX Broadband Wireless Access	3	4	1,2
21.	WiMAX vs LTE	1	4	1,2
Total Contact Hours		**45**		

Course Unitization Plan – Lab

Exp No.	Experiment Name	Required Contact Hours	CLOs Addressed	References Used
1.	Dijkstra's algorithm	3	3	4
2.	RSA Algorithm	3	3	4
3.	Broadcast routing algorithm	3	4	2
4.	Implement the Data Link Layer Framing Method on Character Stuffing	3	2	5
5.	Cyclic Redundancy check (CRC)	3	3	2
6.	Implement a data set of characters of the CRC polynomials	3	3	6
7.	FIFO (First in First out) IPC channels	3	2	6
8.	Round-robin CPU scheduling algorithm	3	3	4
9.	Subnet graph with weights indicating delay between nodes	3	3	1
10.	Congestion control using Leaky bucket algorithm	3	3	1
Total Contact Hours		**30**		

Learning Assessment- Theory

Bloom's Level of Cognitive Task		Theory (30%)				End Semester Exam (50%)
		CLA-1 (5%)	Mid-1 (10%)	CLA-2 (5%)	Mid-2 (10%)	Theory
Level 1	Remember	50%	40%	40%	40%	30%
	Understand					
Level 2	Apply	50%	60%	60%	60%	70%
	Analyse					
Level 3	Evaluate					
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Learning Assessment (Lab)

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		Experiments (20%)	Record / Observation Note (10%)	Viva + Model (20%)	
Level 1	Remember	20%	50%	60%	40%
	Understand				
Level 2	Apply	40%	50%	40%	20%
	Analyse				
Level 3	Evaluate	40%			40%
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Ames Kurose, Keith Ross "Computer Networking: A Top - Down Approach" Pearson; 7th edition, ISBN-10 : 9780133594140
2. 2. Andrew S Tanenbaum "Computer Networks" Pearson Education India; 5th edition, ISBN-10 : 9332518742.
3. 3. Randall Nagy "TCP/IP and UDP/IP for Python 3: Using Python's Internet Protocols", Publisher(s): Apress, ISBN: 9781484294543.
4. 4.Thomas H. Cormen, Charles E. Leiserson, Ronald Rivest, Clifford Stein, "Introduction to Algorithms", ISBN: 978-0-262-04630-5.
5. 5. Behrouz A. Forouzan "Data Communications and Networking", ISBN:9780072967753, 0072967757.
6. 6. Abraham Silberschatz, Peter B. Galvin, Greg Gagne "Operating System Concepts", ISBN: 9781119439257, 1119439256

Other Resources

Course Designers

1. Dr. Karthikeyan E, Assistant Professor, Dept. of ECE. SRM University – AP.

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Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Research Seminar I

Course Code	AEC 502	Course Category	AEC		L	T	P	C
					0	0	1	1
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

1. Survey the existing research works/literature and analyse them.
2. Attain adequate knowledge of a research problem chosen.
3. Improve the presentation/communication skills to articulate their research work.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Review and analyse the existing research work in a systematic way.	3	80%	70%
Outcome 2	Attain strong technical, domain knowledge in the research topic chosen.	3	80%	70%
Outcome 3	Attain good presentation skills to articulate the research problem, analysis and its solution	2	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2				2	2	2	1	3	3	2
Outcome 2	3	2	3				2	1	2	1	3	3	3
Outcome 3	1	1	1			1	2	1	2	1	3	1	1
Average	2	2	3			1	2	2	2	1	3	2	3

Course Unitization Plan

Student is expected to spend minimum 2 hours/week for the Project work.

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)	
		Review -I		Mid Review		Final Review	
		Th	Prac	Th	Prac	Th	Prac
Level 1	Remember		20%		20%		20%
	Understand						
Level 2	Apply		80%		80%		80%
	Analyse						
Level 3	Evaluate						
	Create						
Total			100%		100%		100%

Recommended Resources

1.

Other Resources

1.

Course Designers

1. Dr. Rituparna Chowdhury, Assistant Professor, Dept. of ECE. SRM University – AP
2. Dr. Ramakrishna, Assistant Professor, Dept. of ECE. SRM University – AP

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COMMUNITY SERVICE AND SOCIAL RESPONSIBILITY

Course Code	VAC 502	**Course Category**	VAC	**L**	**T**	**P**	**C**
				0	0	2	2
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	CEL	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. Encourage initiatives that address local needs, foster self-sufficiency, and promote environmental sustainability within the community.
2. Equip participants with a deeper understanding of social issues and a sense of responsibility towards marginalized communities.
3. Inspire active participation in community service programs and foster a culture of giving back among individuals and organizations.
4. Develop and implement programs that contribute to skill development, economic empowerment, and equal opportunities for underprivileged sections of society.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Develop effective strategies for identifying and addressing community needs.	3	80%	80%
Outcome 2	Demonstrate empathy and cultural sensitivity when engaging with diverse community groups.	4	80%	75%
Outcome 3	Implement sustainable solutions and evaluate their impact on social well-being.	5	90%	85%
Outcome 4	Collaborate effectively within teams to design and lead community service projects.	6	90%	80%

Learning Assessment

Bloom's Level of Cognitive Task		**Continuous Learning Assessments 50%**				**End Semester Exam 50%**
		CLA-1 20%	**Mid-1 20%**	**CLA-2 20%**	**CLA-3 20%**	
Level 1	Remember	10%	10%			20%
	Understand					
Level 2	Apply		10%	10%		20%
	Analyse					
Level 3	Evaluate				10%	10%
	Create					
Total		**10%**	**20%**	**10%**	**10%**	**50%**

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Entrepreneurial Mindset

Course Code	SEC 103	Course Category	SEC	L	T	P	C
				1	0	1	2
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)			
Course Offering Department	Management	Professional / Licensing Standards					

Course Objectives / Course Learning Rationales (CLRs)

1. To develop a foundation in innovation and entrepreneurship among the students.
2. To enhance analytical skills of students for practical application of their ideas.
3. To make students proficient in designing solutions.
4. To introduce students to different phases of entrepreneurship.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Describe and classify the basic concepts of Innovation and Entrepreneurship	1	90%	80%
Outcome 2	Discuss the concept of Design Thinking and prototyping	1	80%	70%
Outcome 3	Apply design thinking to generate innovative ideas and strategize implementation plan	2	65%	60%
Outcome 4	Prepare a business plan by assessing customer segment, market validation and product development	2	60%	60%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	1	1							2	3	2	3
Outcome 2	2	2	2	2		2				3	2	2	2
Outcome 3	1	3	3						3		3	2	1
Outcome 4	2	3	3					2	3	3		3	2
Average	2	3	2	1		1		1	2	3	3	3	2

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Entrepreneurship & Inventions**	**5**		
1.	Entrepreneurship and Types of Entrepreneurships	2	1	3,4
2.	Entrepreneurs and their Characteristics	1	1	3,4
3.	Innovation & its Types	2	1	1
Unit 2	**Exploration & Summarizing Facts**	**3**		
4.	Structured exploration and quantifying the data	2	3,4	3,4
5.	Analysing the data	1	3,4	3,4
Unit 3	**Reflection, Synthesizing and ideating**	**3**		
6.	Summarizing facts and designing a workable model	3	3,4	3,4
Unit 4	**Prototyping**	**8**		
7.	Definition and Basics of Prototyping	2	2,3,4	2
8.	Types and methods of Prototyping	4	2,3,4	2
9.	Innovations in prototyping	2	2,3,4	2
Unit 5	**Concept Ideation & Design Thinking**	**8**		
10.	Importance of Idea	1	3,4	1,2
11.	Idea Generation Techniques	1	3,4	1,2
12.	Validating the idea	1	3,4	1,2
13.	Definition and Basics of Design Thinking	2	2	5
14.	Stages of Design Thinking	3	2	5
Unit 6	**Market Validation**	**5**		
15.	Concept of Market Validation and its importance	2	3,4	3,4
16.	Customer survey	1	3,4	3,4,5
17.	Feedback and modifying the idea	2	3,4	3,4,5
Unit 7	**Segmentation of the potential users/ customers**	**3**		
18.	Customer segment and its types	2	4	3,4
19.	Understanding niche customer segment	1	4	3,4
20.	Reaching the real customers	1	4	3,4
Unit 8	**Industry Validation**	**2**		
21.	Industry validation and mentoring	2	3,4	3,4,5
Unit 9	**Solution Design**	**8**		
22.	Generate an Innovative Idea	3	3,4	1,2,5
23.	Develop a Business Plan	5	4	3,4
Total Contact Hours		**45**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		CLA-1 (10%)	CLA-2 (20%)	Mid-term (20%)	
Level 1	Remember	90%	50%	60%	40%
	Understand				
Level 2	Apply	10%	50%	40%	60%
	Analyse				
Level 3	Evaluate				
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Larry Keeley Brian Quinn Ryan Pikkel. Ten types of innovation -the discipline of building breakthroughs, John Wiley& Sons, Inc; 2013
2. Eric Ries. The lean startup how constant innovation creates radically successful businesses, Penguin Books
3. Bruce R. Barringer, R. Duane Ireland. Entrepreneurship Successfully Launching New Ventures, Pearson; 2020
4. Robert D. Hasrich, Dean A. Shepherd, Michael P. Peters, Entrepreneurship, McGraw Hill, 2020
5. Siva Prasad N. Design Thinking : Techniques And Approaches, Ane Books, New Delhi; 2023

Other Resources

Course Designers

1. Mr Udayan Bakshi, Assistant Professor, Paari School of Business, SRM University, A.P.

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IoT Architecture and Protocol

Course Code	IoT 505	**Course Category**	CC	**L**	**T**	**P**	**C**
				3	0	1	4
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. Understand the Architectural Overview of IoT
2. Understand the IoT Reference Architecture and Real World Design Constraints
3. Understand the various IoT Protocols (Datalink, Network, Transport, Session, Service) and its security aspects.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the various IoT Architectures	1	80%	70%
Outcome 2	Understand IoT wireless protocols and the lower layer protocols	1	80%	70%
Outcome 3	Understand and apply the application layer protocols used in IoT.	2	80%	70%
Outcome 4	Understand and use the IoT platform.	1	80%	70%
Outcome 5	Understand the IoT Security concepts.	1	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2				1		1	1	1	3	2
Outcome 2	3	3	2				1		2	2	2	3	2
Outcome 3	3	1	3				1		1	2	2	3	3
Outcome 4	3	1	3				1		2	2	2	3	3
Outcome 5	3	1	3				1		2	2	2	3	3
Average	3	1	2				1		2	2	2	3	2

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**IoT Architecture**	**9**		
1	IoT Architecture – Different layers	2	1	1,3
2	Sensors and Actuators	2	1	1,3
3	Gateways	2	1	1,3
4	Analytics and Data services	1	1	1,3
5	Application layer, Communication Models	1	1	1,3
6	IoT Architecture - Case Study	1	1	1,3
Unit 2	**Lower Layer/Wireless Protocols**	**10**		
7	Zigbee, Zwave, Dash7	1	**2**	1,6
8	Bluetooth Low Energy	2	2	2
9	IEEE 802.11, IEEE 802.15.4, TCP, UDP	3	2	1,6
10	Network Layer-IPv4, IPv6,6LoWPAN, RPL	3	2	1,6
11	Cellular IoT -NB-IoT, LTE-m	1	2	4
Unit 3	**IoT –Application Layer Protocols**	**10**		
12	MQTT	3	3	1,3
13	Hyper Text Transfer Protocol (HTTP)	1	3	1
14	Web sockets, REST	2	3	1
15	CoAP	2	3	1
16	AMCP, XMPP	2	3	1
Unit 4	**IoT Cloud Platforms**	**9**		
17	Various Cloud platforms	1	4	3,5
18	MQTT communication /Data Retrieval	2	4	3
19	Database storage	2	4	3
20	SMS/Email Alert services	2	4	3
21	Data Analytics using algorithm/Serverless computing	2	4	3
Unit 5	**IoT Security**	7		
22	IoT Device/Embedded Security	1	5	5
23	Encryption – Private and Public key Encryption	1	5	5
24	Hash Algorithms, Digital Signature	1	5	5
25	Transport Layer Security - TLS/DTLS	2	5	5
26	Network Layer Security	2	5	5
	Total Contact Hours	**45**		

Course Unitization Plan – Lab

Session	Description of Experiment	Contact hours required	CLOs Addressed	Reference Used
1	TCP Server - Single Client Socket Program (C)	2	2	7
2	TCP Server - Multi Client Socket Program (C)	4	2	7
3	UDP Server - Client Communication (C)	2	2	7
4	HTTP Server (Apache Server) - Web Page and Server side script for MySQL Connectivity (PHP - MySQL)	4	1, 3,4	8
5	HTTP Server with REST API	2	3	9
6	MQTT Publish Subscribe Client with AWS/Mosquitto Broker - Python	4	1, 4,5	11
7	CoAP Server/Client - Arduino - Browser Add on)	4	3	10
8	Bluetooth Low Energy - Notify example with nRF Connect app - (Arduino ESP32)	2	2	12
9	IPV6 TCP Client-Server communication program (C)	2	2	7
10	Contiki /Cooja Demonstration	4	2,3	13
Total Contact Hours		**30**		

Learning Assessment- Theory

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)								End Semester Exam (50%)	
		CLA-1 (15%)		Mid-1 (15%)		CLA-2 (10%)		CLA-III (10%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	70%		70%		60%		50%		60%	
	Understand										
Level 2	Apply	30%		30%		40%		50%		40%	
	Analyse										
Level 3	Evaluate										
	Create										
Total		**100%**		**100%**		**100%**		**100%**		**100%**	

Learning Assessment – Lab

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		Experiments (15%)	Record / Observation Note (10%)	Viva + Model (25%)	
Level 1	Remember	30%	70%	30%	30%
	Understand				
Level 2	Apply	70%	30%	70%	70%
	Analyse				
Level 3	Evaluate				
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Arsheep Bahga, Vijay Madisetti, "INTERNET OF THINGS - A HANDS-ON APPROACH", 1st Edition, Orient Blackswan Private Limited, New Delhi, 2015.
2. Kevin Townsend, Carles Cufí, Akiba, Robert Davidson, "Getting Started with Bluetooth Low Energy", O'Reilly Media, Inc, 2014
3. Agus Kurniawan, "Learning AWS IoT: Effectively manage connected devices on the AWS cloud using services such as AWS Greengrass, AWS button, predictive analytics and machine learning", Packt Publishing, 2018.
4. Cameron Coursey, "The Practitioner's Guide to Cellular IoT", Artech House, 2020.
5. Russell, Brian, and Drew Van Duren. Practical Internet of Things Security, 1 st edition, Packt Publishing Ltd, 2016.
6. Simone Cirani, Gianluigi Ferrari, Marco Picone, "Internet of Things: Architectures, Protocols and Standards", Wiley Publications, 2018.
7. W. Richard Stevens, Bill Fenner, Andrew M. Rudoff, "UNIX Network Programming, Volume 1: The Sockets Networking API", Volume I, 3rd Edition, Addison-Wesley Professional, 2003.
8. https://www.w3schools.com/php/php_mysql_intro.asp
9. https://flask-restful.readthedocs.io/en/latest/
10. https://www.arduino.cc/reference/en/libraries/coap-simple-library/
11. http://www.steves-internet-guide.com/into-mqtt-python-client/
12. Kevin Townsend, Carles Cufí, Akiba, Robert Davidson, "Getting Started with Bluetooth Low Energy", O'Reilly Media, Inc, 2014.
13. http://www.contiki-os.org/

Other Resources

Course Designers

1. Dr Ramakrishnan M. Associate Professor, Department of Electronics and Communication Engineering, SRM University – AP.

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SoC Design for IoT

Course Code	IoT 506	**Course Category**	CC	**L**	**T**	**P**	**C**
				3	0	1	4
Pre-Requisite Course(s)	Microprocessors and Microcontrollers	**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. Understand the basics of SoC Design.
2. Learn the techniques to choose a processor for SoC Implementation.
3. Learn different type of memory blocks used in SoC Design.
4. Understand the bus architecture and Custom SoC Design.
5. Learn the designing methods for customized SoC Design using hardware and software co-design.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand and explain the basics of SoC Design.	1	80%	70%
Outcome 2	Understand the techniques in choosing a best processor for SoC implementation and apply it.	2	80%	70%
Outcome 3	Understand the memory blocks used in SoC Design.	1	80%	70%
Outcome 4	Understand various bus architecture in designing Custom SoCs.	1	80%	70%
Outcome 5	Understand various terminologies using hardware and software co-design for designing customized SoC using suitable Processor.	1	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2				1		1	1	1	3	2
Outcome 2	3	3	3				1		2	2	2	3	3
Outcome 3	3	2	2				1		1	2	2	3	2
Outcome 4	3	2	3				1		2	2	2	3	3
Outcome 5	3	2	2				1		2	2	2	3	2
Average	3	2	2				1		2	2	2	3	2

Course Unitization Plan

Unit No.	Description of Topic	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Introduction and Background**	9		
1	Overview of SoC Design Approach	1	1	1,3
2	SoC design requirements and specifications.	1	1	1,3,4
3	Design integration – design complexity.	1	1	1,3,4
4	Cycle time, die area and cost,	1	1	1,3,4
5	Ideal and practical scaling.	1	1	1,3,4
6	Area-time-power trade-off in processor design.	1	1	1,3,4
7	SoC Design – Behavioural Synthesis	1	1	1,3
8	On-Chip Communication Architecture	1	1	1,3,4
9	Modelling and Co-Simulation	1	1	1,3
Unit 2	**Processor Selection for SoC**	9		
10	Processor architectures	1	2	1
11	Processor core selection.	1	2	1,2
12	Basic concepts – instruction set, branches.	1	2	1,2
13	Interrupts and exceptions.	1	2	1,2
14	Basic elements in instruction handling.	1	2	1,2
15	Minimizing pipeline delays	1	2	1,2
16	Reducing the cost of branches – Robust processors	1	2	1,2
17	Vector processors, VLIW processors	1	2	1,2
18	Superscalar processors.	1	2	1,2
Unit 3	**Memory Design for SOC**	9		
19	Memory and addressing.	1	3	1
20	SoC external memory, SoC internal memory	1	3	1,2,4
21	Scratch pads and cache memory	1	3	1,2,4
22	Cache organization and write policies	1	3	1,2,4
23	Strategies for line replacement at miss time	1	3	1,2,4
24	Split I- and D-Caches	1	3	1,2,4
25	Multilevel Caches	1	3	1,2,4
26	SoC memory systems	1	3	1,2,4
27	Simple processor/memory interaction.	1	3	1,2,4
Unit 4	**Interconnects**	7		
28	System-Level Interconnection	1	4	2
29	Basic Bus Architecture	1	4	2,3
30	SOC Standard Buses – AMBA	1	4	2,3
31	SOC Standard Buses – Core Connect	1	4	2
32	Bus Interface Units	1	4	2
33	Analytical Bus Models	1	4	2
34	Network on Chip	1	4	2,3
Unit 5	**SoC Customization and Case studies**	11		
35	Overview of SoC Customization	1	C	1,3
36	Customizing Instruction Processors	1	C	1,3
37	Customizable Soft Processor	1	C	1,3
38	Case study: AES	2	C	1,3
39	Case study: JPEG Compression	2	C	1,3
40	Case study: Video Compression	2	C	1,3
41	Case study: MP3 Audio Decoding	1	C	1,3
42	Case study: Software Defined Radio	1	C	1,3
	Total contact hours	**45**		

Course Unitization Plan – Lab

Session	Description of Experiment	Contact hours required	CLOs Addressed	Reference Used
1	Design of basic building blocks of the processor using HDL	2	1	5,6
2	Design of basic building blocks of the processor using HDL	2	1	5,6
3	IP Core Creation Using VHDL- Multiplier	2	1,2	5,6
4	IP Core Creation Using VHDL – Adders and Comparator	2	1,2	5,6
5	IP Core Creation Using VIVADO HLS.	2	1,2	5,6
6	IP Core Creation Using MATLAB HDL-Coder.	2	2,3	5,6
7	Creating a Micro Blaze Soft Processor	2	2,3	5,6
8	Designing an Interrupt-based System targeting Xilinx Zynq	2	2	5,6
9	Design a Block RAM Memory with IP using Vivado	2	2	5,6
10	DMA System level Design with custom IP using Vivado	2	2	5,6
11	Generating custom AXI4-Stream IP core using Vivado	2	2	5,6
12	Use of IP cores for DSP applications.	4	2,3	5,6
13	Project	2	2,3	5,6,7
14	Project	2	2,3	5,6,7
Total Contact Hours		**30**		

Learning Assessment -Theory

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)								End Semester Exam (50%)	
		CLA-1 (10%)		Mid-1 (20%)		CLA-II (10%)		CLA-III (10%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	40%		30%		40%		40%		50%	
	Understand										
Level 2	Apply	60%		70%		60%		60%		50%	
	Analyse										
Level 3	Evaluate										
	Create										
Total		100%		100%		100%		100%		100%	

Learning Assessment – Lab

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		Experiments (20%)	Record / Observation Note (10%)	Viva + Model (20%)	
Level 1	Remember	30%	70%	30%	30%
	Understand				
Level 2	Apply	70%	30%	70%	70%
	Analyse				
Level 3	Evaluate				
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”, John Wiley and sons,2011.
2. Rahul Dubey, “Introduction to Embedded System Design Using Field Programmable Gate Arrays”, Springer Verlag London Ltd.,2009.
3. Sudeep Pasricha and Nikil Dutt, On-Chip Communication Architectures - System on Chip Interconnect, Elsevier, 2008.
4. Steve Furber, System-on-chip Architecture, Addison-Wesley, 2000.
5. Xilinx Documentation www.xilinx.com
6. nanoHUB.org - Courses: ECE 695R: System-on-Chip Design: o1a
7. https://www.udemy.com/course/system-on-chip-design-using-vivado-and-zybo-z7-10/?couponCode=KEEPLEARNING

Other Resources

Course Designers

1. Dr Leenendra Chowdary Gunnam. Assistant Professor, Department of Electronics and Communication Engineering, SRM University – AP.

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Wireless Sensor Network and IoT

Course Code	IoT 507	**Course Category**	CC	**L**	**T**	**P**	**C**
				3	0	1	4
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. Acquire comprehensive knowledge of wireless sensor network technologies, including Bluetooth, ZigBee, Wi-Fi, and UWB.
2. Master the fundamentals of MAC protocols, including low duty cycle and wakeup concepts, and apply them in diverse WSN scenarios.
3. Design efficient sensor network architectures based on optimization goals, understanding data dissemination techniques, and incorporating gateways.
4. Implement IP-based WSNs, including 6LOWPAN, and gain practical experience using Tiny OS for WSNs and IoT applications.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Identify and differentiate between various wireless technologies used in WSN, including Bluetooth, ZigBee, and Wi-Fi.	1	75%	70%
Outcome 2	Implement and analyse low duty cycle, contention based, and schedule-based MAC protocols, such as SMAC, BMAC, TRAMA, and IEEE 802.15.4 MAC, to optimize communication in WSN.	1	70%	65%
Outcome 3	Develop strategies for data dissemination, flooding, and gossiping in different WSN scenarios, while setting optimization goals and understanding key figures of merit.	2	85%	70%
Outcome 4	Demonstrate the ability to transition from circuit switching to packet switching, comprehend IPV4, IPV6, and 6LOWPAN concepts, and integrate IP-based WSN with a focus on applications using Tiny OS in IoT and M2M communication.	2	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	1	1	1	1						1	1	1	1
Outcome 2	2	2	3	2				2	1	1	1	2	3
Outcome 3	2	2	2	3							1	2	2
Outcome 4	2	3	3	3				2	1	1	2	2	3
Average	3	2	3	3				2	1	2	2	3	3

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Fundamentals of Wireless Sensor Network (WSN)**	**9**		
1.	Bluetooth, ZigBee, Wi-Fi.	2	1	1, 2
2.	Wireless LAN & PAN, UWB.	2	1	1, 2
3.	Characteristic and challenges.	1	1	1, 2
4.	WSN vs Adhoc Networks.	1	1	1, 2
5.	Sensor node architecture.	1	1	1, 2
6.	Physical layer and transceiver design considerations in WSNs.	1	1	1, 2
7.	Choice of modulation scheme, Dynamic modulation scaling, Antenna considerations.	1	1	1, 2
Unit 2	**WSN (Medium access control)**	**9**		
8.	Fundamentals of MAC protocols - Low duty cycle protocols and wakeup concepts.	2	2	1, 2
9.	Contention Based protocols.	2	2	1, 3
10.	Schedule-based protocols - SMAC – BMAC.	2	2	1, 3
11.	Traffic-adaptive medium access protocol (TRAMA).	2	2	1, 3
12.	The IEEE 802.15.4 MAC protocol.	1	2	1, 3
Unit 3	**Sensor Network Architecture**	**9**		
13.	Data Dissemination, Flooding and Gossiping-Data gathering Sensor Network Scenarios.	1	3	1, 2
14.	Optimization Goals and Figures of Merit	2	3	1, 2
15.	Design Principles for WSNs- Gateway Concepts, Need for gateway.	2	3	1, 2
16.	WSN and Internet Communication	2	3	1, 2
17.	WSN Tunnelling	2	3	1, 2
Unit 4	**IP based WSN**	**9**		
18.	Circuit switching, packet switching.	1	4	1, 2
19.	concept of IPV4, IPV6.	2	4	1, 2
20.	6LOWPAN and IP	2	4	1, 2
21.	IP based WSN.	2	4	1, 2
22.	6LOWPAN based WSN.	2	4	1, 2
Unit 5	**Tiny OS**	**9**		
23.	Tiny OS for WSN	2	4	1, 3
24.	Tiny OS for IoT	2	4	1, 3
25.	M2M communication	1	4	1, 3
26.	AllJoyn network	2	4	1, 3
27.	Contemporary issues and Applications.	2	4	1, 3
Total Contact Hours		**30**		

Course Unitization Plan – Lab

Exp No.	Experiment Name	Required Contact Hours	CLOs Addressed	References Used
1	Sensor Node Deployment over Simulated Testbed	3	1	1
2	Connection Establishment among Sensor Nodes	3	2	1
3	Simulated Wireless Sensor Network Development.	3	2	2
4	Various Network Topology Implementation for WSN.	3	2	2
5	Data Routing over Wireless Sensor Network.	3	3	2
6	Energy Measurement Models and Implementation over WSN.	3	3	2
7	LEACH Protocol Implementation	3	3	1
8	Clustering of Sensor Nodes.	3	4	2
9	Time Synchronization over WSN.	3	4	2
10	Node Localization over WSN	3	4	1
Total Contact Hours				

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		Experiments (20%)	Record / Observation Note (10%)	Viva + Model (20%)	
Level 1	Remember	30%	70%	30%	30%
	Understand				
Level 2	Apply	70%	30%	70%	70%
	Analyze				
Level 3	Evaluate				
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Waltenegus W. Dargie, Christian Poellabauer, "Fundamentals of Wireless Sensor Networks: Theory and Practice", 2014, 1 st ed., John Wiley & Sons, New Jersey
2. Holger Karl, Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks" 2011, 1 st ed., John Wiley & Sons, New Jersey
3. Kazem, Sohraby, Daniel Minoli, Taieb Zanti, "Wireless Sensor Network: Technology, Protocols and Application", John Wiley and Sons 1st Ed., 2007 (ISBN: 978-0-471-74300-2).

Other Resources

1. Jun Zheng, Abbas Jamalipour, "Wireless Sensor Networks: A Networking Perspective", 2014, 1 st ed., Wiley-IEEE Press, USA.

Course Designers

1. Dr. Sunil Chinnadurai. Asst. Professor. Dept. Of ECE. SRM University – AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Project management

Course Code	IOT 501	Course Category	RDIP	L	T	P	C
				0	0	3	3
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)			
Course Offering Department	Mechanical Engineering	Professional / Licensing Standards					

Course Objectives / Course Learning Rationales (CLRs)

1. To understand the fundamentals of production and operations management.
2. To learn about capacity planning, plant layout, scheduling and sequencing
3. To learn about operation management, work study, time study
4. To understand about Inventory control, supply chain management

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Define and explain the basic concepts and principles of production and operations management (POM),	1	80%	75%
Outcome 2	Develop proficiency in capacity planning, plant layout etc.	2	70%	75%
Outcome 3	Able to perform work study, time study, Gantt chart	2	80%	70%
Outcome 4	Explain supply chain management functions and applications	2	80%	75%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	1	3	2				3		3	3	2	3
Outcome 2	3	2	3	2				3		3	3	2	3
Outcome 3	3	2	3	2				3		3	3	2	3
Outcome 4	3	3	3	2				3		3	3	3	3
Average	3	2	3	2				3		3	3	2	3

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
UNIT-I	**Fundamental concepts**	**8**		
1.	Production planning and control	2	1	1
2.	New product development	1	1	1,2
UNIT-II	**Plant layout**	**8**		
3.	Capacity planning, facility planning	2	1	1
4.	Plant location and layout	2	1,2	1,2
5.	Scheduling and sequencing	2	1,2	1,2
UNIT- III	**Operation management**	**9**		
6.	CPM	3	3	1
7.	Gantt chart	3	3	2
8.	Work study, time study	3	3	1,2
UNIT-IV	**Material management**	**10**		
9.	ABC analysis, EOQ	3	3,4	1
10.	Supply chain management	4	3,4	1
11.	Preventive maintenence	3	3,4	2
UNIT – V	**Tools**	**10**		
12.	Six sigma, Poka yoke, BPR, ERP, Kanban, ISO 9000,	5	3,4	2
13.	JIT, TQM, FMS, Push/Pull, Kaizen, CAD CAM	5	3,4	2
Total Contact hours		**45**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)	
		Assignment-I		Assignment -II			
		Th	Prac	Th	Prac	Th	Prac
Level 1	Remember		20%		20%		20%
	Understand						
Level 2	Apply		80%		80%		80%
	Analyse						
Level 3	Evaluate						
	Create						
Total			100%		100%		100%

Recommended Resources

1. Bhattacharyya, "Production and Operations Management", Universal Press , Edition
2. Panneer selvam R; "Production and Operations Management", Prentice Hall of India, Edition

Other Resources

Course Designers

1. Prof. Prakash Jadhav, Professor, Department of Mechanical Engineering, SRM university AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Research Seminar- II

Course Code	AEC 503	Course Category	AEC		L	T	P	C
					0	0	1	1
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

1. Survey the existing research works/literature and analyse them.
2. Attain adequate knowledge of a research problem chosen.
3. Improve the presentation/communication skills to articulate their research work.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Review and analyse the existing research work in a systematic way.	2	80%	70%
Outcome 2	Attain strong technical, domain knowledge in the research topic chosen.	2	80%	70%
Outcome 3	Attain good presentation skills to articulate the research problem, analysis and its solution	1	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2				2	2	2	1	3	3	2
Outcome 2	3	2	3				2	1	2	1	3	3	3
Outcome 3	1	1	1			1	2	1	2	1	3	1	1
Average	2	2	3			1	2	2	2	1	3	2	3

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1				
Unit 2				
Unit 3				
Unit 4				
Unit 5				

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)	
		Review -I		Mid Review		Final Review	
		Th	Prac	Th	Prac	Th	Prac
Level 1	Remember		20%		20%		20%
	Understand						
Level 2	Apply		80%		80%		80%
	Analyse						
Level 3	Evaluate						
	Create						
Total			100%		100%		100%

Recommended Resources

Other Resources

Course Designers

1. Dr. Ramakrishnan, Associate Professor, Dept. of ECE. SRM University – AP.
2. Dr. Rituparna Chowdhury, Assistant Professor, Dept. of ECE. SRM University – AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Thesis - I

Course Code	IoT 509	Course Category	RDIP	L	T	P	C
				0	0	14	14
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)			
Course Offering Department	ECE	Professional / Licensing Standards					

Course Objectives / Course Learning Rationales (CLRs)

1. Survey the existing research works/literature and analyze them.
2. Demonstrate the skills acquired to solve a technical problem.
3. To have a systematic approach to solve the given problem.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Review and analyze the existing research work systematically.	1	80%	70%
Outcome 2	Attain strong technical, and domain knowledge in the field of project.	2	80%	70%
Outcome 3	Formulate the complex problem and have a systematic approach for the solution.	2	80%	70%
Outcome 4	Conduct research project	2	80%	70%
Outcome 5	Communicate the technical problems with peers and mentors to move towards appropriate solutions.	2	75%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2				2	2	2	1	3	3	2
Outcome 2	3	3	3			1	2	1	2	1	3	3	3
Outcome 3	2	2	3	1	1	1	2	1	2	1	3	2	3
Outcome 4	2	2	3	1	1	1	2	2	3	1	3	2	3
Outcome 5	2	2	3	1	1	1	2	3	3	1	3	2	3
Average	2	2	3	1	1	1	2	2	2	1	3	2	3

Course Unitization Plan

The student is expected to spend a minimum of 12 hours/week on the Project work

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)	
		Review -I		Mid Review		Final Review	
		Th	Prac	Th	Prac	Th	Prac
Level 1	Remember		20%		20%		20%
	Understand						
Level 2	Apply		80%		80%		80%
	Analyse						
Level 3	Evaluate						
	Create						
Total			100%		100%		100%

Recommended Resources

Other Resources

Course Designers

1. Dr. Ramakrishanan Maharajan, Department of Electronics and Communication Engineering, SRM University - AP

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Industrial Practice

Course Code	IoT 510	**Course Category**	RDIP	**L**	**T**	**P**	**C**
				0	0	3	3
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department		**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1				
Outcome 2				
Outcome 3				
Outcome 4				

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1													
Outcome 2													
Outcome 3													
Outcome 4													
Outcome 5													
Average													

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1				
Unit 2				
Unit 3				
Unit 4				
Unit 5				

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		CLA-1 20%	Mid-1 20%	CLA-2 20%	CLA-3 20%	
Level 1	Remember					
	Understand					
Level 2	Apply					
	Analyse					
Level 3	Evaluate					
	Create					
Total						

Recommended Resources

Other Resources

Course Designers

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Thesis - II

Course Code	IoT 511	Course Category	RDIP			L	T	P	C
						0	0	15	15
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)					
Course Offering Department	ECE	Professional / Licensing Standards							

Course Objectives / Course Learning Rationales (CLRs)

1. Survey the existing research works/literature and analyse them.
2. Demonstrate the skills acquired to solve a technical problem.
3. To have systematic approach to solve the given problem.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Review and analyse the existing research work in a systematic way.	1,2	80%	70%
Outcome 2	Attain strong technical, domain knowledge in the field of project.	2	80%	70%
Outcome 3	Formulate the complex problem and to have systematic approach for the solution.	2	80%	70%
Outcome 4	Conduct research project	2	80%	70%
Outcome 5	Communicate the technical problems with peers and mentors to move towards appropriate solution.	1	75%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2				2	2	2	1	3	3	2
Outcome 2	3	3	3			1	2	1	2	1	3	3	3
Outcome 3	2	2	3	1	1	1	2	1	2	1	3	2	3
Outcome 4	2	2	3	1	1	1	2	2	3	1	3	2	3
Outcome 5	2	2	3	1	1	1	2	3	3	1	3	2	3
Average	2	2	3	1	1	1	2	2	2	1	3	2	3

Course Unitization Plan

The student is expected to spend at least 32 hours/week on the Project work.

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)	
		Review -I		Mid Review		Final Review	
		Th	Prac	Th	Prac	Th	Prac
Level 1	Remember		20%		20%		20%
	Understand						
Level 2	Apply		80%		80%		80%
	Analyse						
Level 3	Evaluate						
	Create						
Total			100%		100%		100%

Recommended Resources

Other Resources

Course Designers

1. Dr. Ramakrishanan Maharajan, Department of Electronics and Communication Engineering, SRM University – AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Designing Embedded Systems using UML

Course Code	IoT 532	**Course Category**	CE	**L**	**T**	**P**	**C**
				3	1	0	4
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To Understand the UML diagrams used in modelling.
2. To understand an agile development process and to describe the various industry standards for the software design.
3. To understand the application of UML to model and design distributed concurrent systems

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the various UML Diagrams	1	80%	70%
Outcome 2	Understand the embedded software development process and workflow.	1	80%	70%
Outcome 3	Capture the System Requirements and organize the system model.	2	80%	70%
Outcome 4	Understand and apply the design patterns	2	80%	70%
Outcome 5	Understand the modelling of concurrent, distributed systems.	1	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	1				1		1	1	1	3	1
Outcome 2	3	2	2				1		2	1	1	3	2
Outcome 3	3	2	2				1		1	2	2	3	2
Outcome 4	3	2	2				1		2	2	2	3	2
Outcome 5	3	2	2				1		2	2	2	3	2
Average	3	2	2				1		2	2	2	3	2

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
UNIT I	**Introduction to UML**	**9**		
1.	UML Basic Modelling concepts	1	1	1,5
2.	Structural Elements and Diagrams	1	1	1,5
3.	Objects, Classes and Interfaces	1	1	1,5
4.	Relations	1	1	1,5
5.	Subsystems, components, and Packages	1	1	1,5
6.	Behavioural elements and diagrams	1	1	1,5
7.	Action and Activities	1	1	1,5
8.	Operations and methods	1	1	1,5
9.	State Diagrams, Interactions	1	1	1,5
UNIT II	**Development Process**	**9**		
10.	Harmony Development Process	1	2	1
11.	Need for Process, Harmony process overview	1	2	1
12.	System Engineering Harmony workflow	1	2	1
13.	System Functional Analysis	1	2	1
14.	Use Case Model Workflow	1	2	1
15.	The Hand-off from system engineering	1	2	1
16.	Software workflow, Analysis and Design	1	2	1
17.	Verification and Validation	1	2	1
UNIT III	**System Requirements and Architecture**	**9**		
17.	Representing requirements on UML and SysML	2	3	1
18.	State Machines for Requirement capture	1	3	1
19.	System Architecture	1	3	1
20.	Organizing the system Model	1	3	1
22.	Subsystem identification	1	3	1
21.	Mapping Operational contracts into sub system architecture	2	3	1
22.	Identification of sub system use cases	1	3	1
UNIT IV	**Design Patterns and Modelling**	**9**		
23.	Design patterns	1	4	1,2
24.	Basic Structures of Design Patterns	1	4	1,2
25.	Using Design Patterns in Development	2	4	1,2
26.	Design for Safety, Reliability and Security	1	4	1
27.	High Fidelity Modelling	1	4	1
28.	Structured Design with UML	1	4	1
29.	Modelling Workflow	1	4	1
30.	Object Identification	1	4	1
UNIT V	**Distribution, Concurrency and Resource Architecture**	**9**		
31.	Asymmetric and Symmetric Distributed Architecture	1	5	1
32.	Concurrency and Resource Architecture	2	5	1,2,3,4
33.	Concurrency Architecture Harmony Workflow	1	5	1,2,3,4
34.	Concurrency Problems	2	5	1,2,3,4
35.	Collaboration Design	2	5	1
36.	Detailed Design	1	5	1
Total Contact Hours		**45**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)								End Semester Exam (50%)	
		CLA-1 (15%)		Mid-1 (15%)		CLA-2 (10%)		CLA-III (10%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	70%		70%		60%		70%		60%	
	Understand										
Level 2	Apply	30%		30%		40%		30%		40%	
	Analyse										
Level 3	Evaluate										
	Create										
Total		**100%**		**100%**		**100%**		**100%**		**100%**	

Recommended Resources

1. Bruce Powel Douglass, "Real-Time UML Workshop for Embedded Systems", 2nd Edition, Newnes, 2014Peter Waher, "Learning Internet of Things", Packt Publishers, 2015
2. Lavagno, Luciano, Martin, Grant, Selić, Bran (Eds.), "UML for Real, Design of Embedded Real-Time Systems", Springer, US, 2003
3. Bran Selic, Sebastien Gerard, "Modeling and Analysis of Real-Time and Embedded Systems with UML and MARTE: Developing Cyber-Physical Systems", The MK/OMG Press,2013.
4. Miro Samek, "Practical UML Statecharts in C/C++: Event-Driven Programming for Embedded Systems", Newnes, 2008.
5. Joseph Schmuller, "Sams Teach Yourself UML in 24 Hours", Third Edition, Sams Publishing, 2004.

Other Resources

Course Designers

1. Dr Ramakrishnan M. Associate Professor, Department of Electronics and Communication Engineering, SRM University – AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Hardware security for IoT

Course Code	IoT 543	**Course Category**	CE	**L**	**T**	**P**	**C**
				3	1	0	4
Pre-Requisite Course(s)	Digital Circuits/Digital Electronics	**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To Understand the basic concepts of various levels of IoT security issues and countermeasures
2. To Design and simulate emerging circuit/architecture countermeasures for improving security.
3. To make students understand the side channel attacks such as power and EM attacks and techniques for prevent SCA's.
4. Design and verification of cryptographic hardware for different fault attacks.
5. Design systems to minimize or prevent various forms of trojans.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Have strong understanding of the basic concepts of various levels of IoT layer security issues and countermeasures	1	80%	70%
Outcome 2	Design and simulate emerging circuit/architecture countermeasures like PUF/TRNG designs for improving hardware security	2	70%	60%
Outcome 3	Design and verify cryptographic algorithms on hardware for various attacks	2	80%	70%
Outcome 4	Well understand and can design the side channel attacks such as power and EM attacks and techniques to prevent such SCA's	2	70%	60%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	1	3				2		2	3	2	3	3
Outcome 2	3	2	3				3		2	3	2	3	3
Outcome 3	3	2	3				2		2	3	2	3	3
Outcome 4	3	3	3				3		2	3	2	3	3
Average	3	2	3				3		2	3	2	3	3

Course Unitization Plan

Session	Description of Topic	Required Contact hours	CLOs addressed	References used
	UNIT I: Overview of IoT security and hardware security	**8**		
1.	IoT system and building blocks,	1	1	1,2,3
2.	Network, Data, software and Hardware security basics	2	1	1,2,3
3.	Introduction to Cryptography	1	1	1,2,3
4.	Block Ciphers Rijndael in Composite Field	2	1	1,2,3
5.	Elliptic Curves	2	1	1,2,3
6.	Scalar Multiplications	2	1	1,2,3
7.	Montgomery's Algorithm for Scalar Multiplication	2	1	1,2,3
a.	**UNIT II: Hardware Design of Cryptographic Algorithms for IoT**	**10**		
8.	Hardware Design of the Advanced Encryption Standard (AES)	2	1,3	1,2,3
9.	Algorithmic and Architectural Optimizations for AES Design	1	1,3	1,2,3
10.	Circuit for the AES S-Box	1	1,3	1,2,3
11.	An Example Reconfigurable Design for the Rijndael Cryptosystem	1	1,3	1,2,3
12.	Design of Finite Field Arithmetic on FPGAs	1	1,3	1,2,3
13.	Finite Field Multipliers for High Performance Applications	1	1,3	1,2,3
14.	Karatsuba Multipliers for Elliptic Curves	1	1,3	1,2,3
15.	Designing for the FPGA Architecture	1	1,3	1,2,3
16.	Elliptic Curve Cryptoprocessor	1	1,3	
a.	**UNIT III**: **Side-channel Attacks on Cryptographic Hardware for IoT**	**10**		
17.	Introduction to Side Channel Analysis and different Attacks: Power, EM attacks	2	1,2,4	1,2,3
18.	Current-measurement based Side-channel Attacks (Case Study: Kocher's Attack on DES),	2	1,2,4	1,2,3
19.	Design Techniques to Prevent Side-channel Attacks,	2	1,2,4	1,2,3
20.	Improved Side-channel Attack Algorithms (Template Attack, etc.)	2	1,2,4	1,2,3
21.	Cache Attacks	2	1,2,4	1,2,3
a.	**UNIT IV: Testability and Verification of Cryptographic Hardware and Modern IC Design and Manufacturing Practices and Their Implications for IoT**	**9**		
22.	Fault-tolerance of Cryptographic Hardware	1	1,2,4	1,2,3
23.	Fault Attacks, Verification of Finite-field Arithmetic Circuits	1	1,2,4	1,2,3
24.	Hardware Intellectual Property (IP) Piracy and IC Piracy	1	1,2,4	1,2,3
25.	Design Techniques to Prevent IP and IC Piracy	1	1,2,4	1,2,3
26.	Using PUFs to prevent Hardware Piracy	1	1,2,4	1,2,3
27.	Model Building Attacks on PUFs (Case Study: SVM Modeling of Arbiter PUFs	2	1,2,4	1,2,3
28.	Genetic Programming based Modeling of Ring Oscillator PUF)	1	1,2,4	1,2,3
a.	**UNIT V: Hardware Trojans and Detection methods for IoT platforms**	**9**		
29.	Hardware Trojans: Hardware Trojan Nomenclature	1	1,2,3,4	1,2,3
30.	Countermeasures Such as Design and Manufacturing Techniques to Prevent/Detect Hardware Trojans,	1	1,2,3,4	1,2,3
31.	Logic Testing and Side-channel Analysis based Techniques for Trojan Detection,	2	1,2,3,4	1,2,3
32.	Techniques to Increase Testing Sensitivity Infrastructure Security	1	1,2,3,4	1,2,3
33.	Impact of Hardware Security Compromise on Public Infrastructure	1	1,2,3,4	1,2,3
34.	Défense Techniques (Case Study: Smart-Grid Security)	2	1,2,3,4	1,2,3
	Total contact hours	**45**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)								End Semester Exam (50%)	
		CLA-1 (5%)		Mid-1 (10%)		CLA-2 (10%)		Mid-2 (20%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	20%		40%		20%		20%	30%	40%	25%
	Understand										
Level 2	Apply	80%		60%		80%		80%	70%	60%	70%
	Analyse										
Level 3	Evaluate										5%
	Create										
Total		**100%**		**100%**		**100%**		**100%**		**100%**	

Recommended Resources

1. Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, "Hardware Security: Design, Threats, and Safeguards", CRC Press.
2. Swarup Bhunia and Mark Tehranipoor, "Hardware Security: A Hands-on Learning Approach", 2019 Elsevier
3. Doug Stinson, Cryptography Theory and Practice, CRC Press

Other Resources

Course Designers

1. Internal (Institutional) Subject Matter Experts
2. Dr Ramesh Vaddi, Associate Professor, Department of Electronics & Communication Engineering, SRM University – AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Deep Learning for IOT

Course Code	IoT 558	**Course Category**	CE	**L**	**T**	**P**	**C**
				3	0	1	4
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To familiarize the domain of fully connected neural networks.
2. To understand and design convolutional neural networks.
3. To understand and design recurrent neural networks.
4. To understand autoencoders and generative models.
5. To have a basic understanding of applications of deep learning

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Design fully connected neural networks	2	85%	80%
Outcome 2	Apply and analyse convolutional neural networks	2	80%	75%
Outcome 3	Apply recurrent neural networks	2	85%	70%
Outcome 4	Apply autoencoders and generative models.	2	80%	70%
Outcome 5	Understand the applications of deep learning	1	75%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	1	1	1						1	1	1	1	1
Outcome 2	2	2	3				2	1	1	2	3	2	3
Outcome 3	2	2	2				2	1	1	2	2	2	2
Outcome 4	2	3	3				2	1	1	3	3	2	3
Outcome 5	3	2	3				2	1	2	2	2	3	3
Average	2	2	3				2	1	1	2	2	2	3

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Introduction to neural network**	**10**		
	Introduction to Neural network	1	1	1, 2
	Feedforward Neural networks	1	1	1, 2
	Gradient descent algorithm	1	1	1, 2
	Back propagation algorithm	1	1	1, 2
	Activation function	1	1	1, 2
	Training neural network	1	1	1, 2
	Risk minimization, loss function	1	1	1, 2
	Regularization and model selection	1	1	1, 2
	Optimization and hyperparameters	1	1	1, 2
	Shallow neural networks and Deep neural networks	1	1	1, 2
Unit 2	**Convolutional neural networks**	**10**		
	Introduction to CNN	1	2	1, 2
	Convolutions and Pooling	1	2	1, 2
	Invariance, stability	1	2	1, 2
	Understanding ConvNets via Visualization	1	2	1, 2
	ConvNet Architectures	2	2	1, 2
	CNN on ImageNet	1	2	1, 2
	Overfitting Bias/Variance trade-off	1	2	1, 2
	Deep Convolutional Neural Networks	2	2	1, 2
Unit 3	**Recurrent neural networks**	**9**		
	Introduction to Recurrent Networks	1	3	1, 2
	Back propagation through time	1	3	1, 2
	The problem of Exploding and Vanishing Gradients	2	3	1, 2
	Long Short Term Memory (LSTM)	2	3	1, 2
	Gated Recurrent Units (GRUs)	1	3	1, 2
	How LSTMs avoid the problem of vanishing gradients	2	3	1, 2
Unit 4	**Autoencoders**	**9**		
	Introduction to Autoencoders	1	4	1, 2
	Introduction to Encoder and Decoder models	1	4	1, 2
	Link between PCA and Autoencoders	1	4	1, 2
	Regularization in autoencoders	1	4	1, 2
	Denoising Autoencoders	1	4	1, 2
	Sparse Autoencoders	1	4	1, 2
	Introduction to Generative Adversarial Networks (GAN)	1	4	1, 2
	Introduction to Reinforcement Learning	2	4	1, 2
Unit 5	**Applications of Deep Learning**	**7**		1, 2
	Introduction	2	5	1, 2
	Data mining	2	5	1, 2
	Big data in health care industries	2	5	1, 2
	Sound/ audio analysis using deep learning techniques	1	5	1, 2
Total Contact Hours		**45**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)								End Semester Exam (50%)	
		CLA-1 (10%)		Mid-1 (15%)		CLA-2 (10%)		CLA-3 (15%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	40%		60%		40%		60%		30%	
	Understand										
Level 2	Apply	60%		40%		60%		40%		70%	
	Analyze										
Level 3	Evaluate										
	Create										
Total		100%		100%		100%		100%		100%	

Learning Assessment- Lab

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		Experiments (15%)	Record / Observation Note (10%)	Viva + Model (25%)	
Level 1	Remember	30%	70%	30%	30%
	Understand				
Level 2	Apply	70%	30%	70%	70%
	Analyse				
Level 3	Evaluate				
	Create				
Total		100%	100%	100%	100%

Recommended Resources

1. Ravichandiran, S., 2019. Hands-On Deep Learning Algorithms with Python: Master deep learning algorithms with extensive math by implementing them using TensorFlow. Packt Publishing Ltd..
2. Goodfellow, I., Bengio, Y., Courville, A. and Bengio, Y., 2016. Deep learning (Vol. 1). Cambridge: MIT Press.

Other Resources

Course Designers

1. Dr. Sudhakar Tummala. Asst. Professor. Dept. Of ECE. SRM University – AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Hardware Accelerators for IoT edge computing

Course Code	IOT 531	**Course Category**	CE	**L**	**T**	**P**	**C**
				3	0	1	4
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To understand DNN structures, Opportunities and Challenges with custom HW Accelerators and recent developments in DNN hardware/Chip Designs from various leading companies
2. To understand how DNN computations are mapped to various hardware platforms and understand the tradeoffs between various architectures/platforms and being able to evaluate different DNN accelerator implementations with benchmarks and performance comparison metrics
3. To get familiar with emerging techniques for processing DNNs on edge devices such as Approximate Computing for DNNs, Precision scalable architectures and emerging NVMs for DNNs.
4. To understand and get hands on implementing various DNN architectures on hardware like CPU, GPU, FPGA, ASIC, etc.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Clearly understand what are DNNs, models, datasets and architectures	1	70%	65%
Outcome 2	evaluate the key design considerations for efficient DNN processing and understand tradeoffs between various hardware architectures and platforms	2	70%	65%
Outcome 3	Understand and implement emerging techniques for processing DNNs on edge devices such as Approximate Computing for DNNs, Precision scalable architectures and emerging NVMs for DNNs, CiM	1,2	70%	65%
Outcome 4	Implement various models on hardware platforms	2	70%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	3	3	1		2				3	3	1	2
Outcome 2	3	3	3	2	1	2		3		2	3	2	2
Outcome 3	3	3	3	2		2		3		3	3	2	2
Outcome 4	3	3	3	2	1	2		3		2	3	2	2
Average	2.4	2.4	2.4	1.4	1	1.6		3		2	2.4	1.4	1.6

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Introduction to Hardware accelerators, IoT Edge Computing, DNNs and Applications**	**8**		
1.	Overview of ML/Deep Learning and Applications,	2	1	1,2,3
2.	Training vs Inference, IoT Embedded vs Cloud Computing	2	1	1
3.	Overview of DNN Components, DNN layers, Popular types of Deep Neural Networks-FN,CNNs, RNNs, LSTM,	2	1	1
4.	Light weight NN Models	2	1	1,2
Unit 2	**DNN models**	**10**		
6.	Popular DNN models	2	1,2	1
7.	HW-SW Co-Design	2	1,2	1
8.	CNNs and implementation	3	1,2	1
9.	DNN development resources	3	1,2	1
Unit 3	**DNN key metrics, Design objectives, hardware platforms**	**10**		
10.	Accuracy, Throughput, Latency	2	2,3,4	1
11.	Power, energy, flexibility, scalability	3	2,3,4	1
12.	Designing DNN accelerators	2	2,3,4	1
13.	Accelerating DNNs in Hardware: study and analysis of various recent platforms on CPU, GPU, FPGA, ASIC platforms	3	2,3,4	1
14.	Architectures of Google's TPU, Apple's Neural Engine, ARM's Project Trillium, etc	2	2,3,4	1
Unit 4	Review of Python & Verilog for FPGA, CAD Tools for ASIC implementations	9		
15.	Review of Python for DNNs with examples	3	2,3,4	1
16.	Review and design of DNNs with HDLs	3	2,3,4	1
17.	Review of cadence EDA based system design for DNNs	3	2,3,4	1
Unit 5	Emerging Techniques for DNN processing on edge devices	**8**		
18.	Precision scalable architectures	2	3	1
19.	Approximate Computing techniques	2	3	1
20.	In-memory computing architectures	2	3	1
21.	Emerging NVMs for DNN processing	2	3	1
	Total	**45**		

Course Unitization Plan - Lab

Exp No.	Experiment Name	Required Contact Hours	CLOs Addressed	References Used
1.	Edge Detection Using Image and Google Colab	4	2,3,4	1, 2
2.	Hardware Implementation of Edge detection using NVIDIA Jetson Nano	2	2,3,4	1, 2
3.	MNIST Digit Classification with a CNN	2	2,3,4	1, 2
4.	Image Classification using CNNs	2	2,3,4	1, 2
5.	Hyperparameter Tuning for Image Classification	2	2,3,4	1, 2
6.	Object Detection and Implementation with Raspberry PI	2	2,3,4	1, 2
7.	Analyses of Interface Time Through Object Detection	2	2,3,4	1, 2
8.	FPGA Implementation of CNNs for Image classification	4	2,3,4	1, 2
9.	Design and Implementation of Precision Scalable architecture, Approximation circuits for DNNs	4	2,3,4	1, 2
10.	Course project Implementation	6	2,3,4	1, 2
Total Contact Hours		**30**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)								End Semester Exam (50%)	
		CLA-1 (10%)		Mid-1 (15%)		CLA-2 (10%)		CLA-3 (15%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	80%	30%	50%	30%	20%	30%	20%	30%	20%	30%
	Understand										
Level 2	Apply	20%	70%	50%	70%	80%	70%	80%	70%	80%	70%
	Analyse										
Level 3	Evaluate										
	Create										
Total		**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Vivienne Sze , Yu-Hsin Chen , Tien-Ju Yang, Joel S. Emer, Efficient Processing of Deep Neural Networks, Springer, 2020. https://link.springer.com/book/10.1007/978-3-031-01766-7
2. Deep Learning by Ian Goodfellow and Yoshua Bengio and Aaron Courville, MIT Press, https://www.deeplearningbook.org/
3. Neural Networks and Deep Learning, http://neuralnetworksanddeeplearning.com

Other Resources

Course Designers

1. Dr. Ramesh Vaddi, Associate Professor, Dept of ECE, SRM University - AP

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

FPGA Design for Embedded systems

Course Code	IoT 530	**Course Category**	CE	**L**	**T**	**P**	**C**
				3	0	1	4
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To introduce the internal architecture of programmable logic with focus on FPGA.
2. To provide knowledge in FPGA design flow at the architectural and system design.
3. To impart a good background in block-based design using standard system level tools

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Ability to understand the structure of the fabric of programmable logic	1	80%	75%
Outcome 2	Implement ideas on Placement and Partitioning of Circuits	2	80%	75%
Outcome 3	Identify concepts and Algorithms of Floor planning and Routing	1	80%	75%
Outcome 4	Develop circuit level techniques and apply in logic Synthesis	2	80%	75%
Outcome 5	Working on High Level Synthesis of Circuits	2	80%	75%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	3	3	1		2	1			3	3	1	2
Outcome 2	3	3	3	2	1	2	1	3		2	3	2	2
Outcome 3	3	3	3	2		2	1	3		3	3	2	2
Outcome 4	3	3	3	2	1	2	1	3		2	3	2	2
Outcome 5	3	3	3	2	1	2	1	2		2	3	2	2
Average	**3**	**3**	**3**	**2**	**1**	**2**	**1**	**3**		**2**	**3**	**2**	**2**

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Programmable Logic Devices**	**10**		
	PROM - PAL - PLA - CPLD - Gate Arrays - MPGA	3	1	1
	FPGA - Programming Technologies - EPROM - EEPROM - FLASH - SRAM - FPGA Fabric	2	1	1
	Configurable Logic Block - LUT - Slice - Slicem	2	1	1
	Programmable Interconnects - Input Output Blocks - Keeper Circuit - Xilinx 7 Series Architecture.	3	1	1
Unit 2	**FPGA Design Flow and Abstraction Levels**	**8**		
	Verilog Design for Synthesis	2	2	1
	One Hot Encoding - Memory Blocks - Block Memory Generator (BRAM/BROM)	2	2	1
	Single Port Memory - Dual Port Memory	2	2	2
	FIFO - Distributed RAM - Synthesis Pitfalls - Latch Inference	2	2	2
Unit 3	**Static Timing Analysis**	**8**		
	Speed Performance - Timing Constraints	2	3	2
	Clock Management - Clock Buffers.	3	3	2
	Clock Tree Routing	3	3	2
Unit 4	**Introduction to SoC Design**	**9**		
	Hard Macros - Multipliers - DSP Block	3	4	3
	Hard Core Processors - Interface Circuits	3	4	3
	Configuration Chain - JTAG Interface - Zynq7000 Architecture	3	4	3
Unit 5	**Timing Simulation and Programming**	**10**		
	Timing Simulation using Modelsim/Icarusverilog,	2	5	3
	Programming using JTAG, System Level testing and debugging	3	5	3
	Debugging techniques	2	5	3
	Debugging using chip scope and Logic analyzers, Protocols on FPGA	3	5	3
	Total Contact Hours	**45**		

Course Unitization Plan – Lab

Session	Description of Experiment	Contact hours required	CLOs Addressed	Reference Used
1.	Introduction to Edge Zynq SoC FPGA Development Board. (Lab Experiment - 1)	1	1	4
2.	Controlling LED in Edge Zynq SoC FPGA Development Board. (Lab Experiment - 2)	2	1	4
3.	1. Designing Combinational Logic circuits Edge Zynq SoC FPGA Development Board. (Lab Experiment - 3)	3	2	5
4.	Designing Sequential Logic circuits Edge Zynq SoC FPGA Development Board. (Lab Experiment - 4)	3	2	5
5.	Control relay using switch on the Edge Zynq Board. (Lab Experiment - 5)	3	3	5
6.	Produce sound at piezo Buzzer at regular interval on Edge Zynq Board. (Lab Experiment - 6)	3	3	5
7.	LDR Interface using ADC. (Lab Experiment - 7)	3	3	5
8.	2x16 Liquid Crystal Display Interface. (Lab Experiment - 8)	3	4	4
9.	4-bit BCD to Seven Segment Display. (Lab Experiment - 9)	3	4	4
10.	Seven Segment Display Counter. (Lab Experiment - 10)	2	5	3
11.	Displays 128x160 pixel image on the SPI TFT Display interfaced to Edge board. (	2	5	4
12.	Project			
Total Contact Hours		**30**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)								End Semester Exam (50%)	
		CLA-1 (10%)		Mid-1 (15%)		CLA-2 (10%)		CLA3 (15%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	60%	30%	50%	40%	60%	30%	50%	40%	50%	50%
	Understand										
Level 2	Apply	40%	50%	50%	50%	40%	60%	50%	50%	40%	40%
	Analyze										
Level 3	Evaluate		20%		10%		10%		10%	10%	10%
	Create										
Total		**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Amano, Hideharu, Principles and Structures of FPGAs, First Edition, Springer, 2018.
2. Readler, Blaine C., Verilog by example: a concise introduction for FPGA design, Full Arc Press, 2011.
3. ZainalabedinNavabi, Embedded Core Design with FPGAs, First Edition, McGraw Hill, 2008.
4. Xilinx Inc, Vivado Design Suite User Guide, 2021.

Other Resources

Course Designers

1. Dr. Saswat Kumar Ram, Assistant Professor, Dept of ECE, SRM University - AP
2. Expert Reviewers from Institutes of National Importance / Institutes of International Repute
3. Expert Reviewers from Industry