Department of Electronics and Communication Engineering

M.Tech. VLSI Curriculum and Syllabus (Applicable to the students admitted from AY: 2023 onwards)



School of Engineering and Sciences SRM University *AP*, Andhra Pradesh



Department Vision

To be a globally recognized leader in the field of Electronics and Communications, by fostering innovation through cutting-edge collaborative research to inform interdisciplinary education.

Department Mission

- 1. Create inclusive and highly motivated individuals and leaders who promote diversity, innovation, creativity, and a high sense of responsibility towards societal progress.
- 2. Strive for excellence by promoting interdisciplinary education and research through global collaborations.
- 3. Deliver state-of-the-art research-based education that equips students with the skills to address contemporary challenges and contribute to the field's advancement.
- 4. Foster a culture of innovation and entrepreneurship, by working closely with leading industry partners to translate ideas into real-life solutions.
- 5. Aim to be a global knowledge hub by collaborating with leading institutions and industries.

Program Educational Objectives (PEO)

- 1. Enable the postgraduate students to learn the fundamentals of VLSI deeply and lay a strong foundation for their professional careers or higher studies.
- 2. Train the students to have hands-on VLSI System design skills which can be applied to solve industrial and research problems in an interdisciplinary environment.
- **3.** Train the students to have comprehensive knowledge and skills in VLSI technologies which can be applied to the given problems in industrial and research multi-disciplinary environments.
- 4. Facilitate the development of effective communication skills, lifelong learning, leadership qualities and ethical professional conduct across their higher education and career paths.

Mission of the Department to Program Educational Objectives (PEO) Mapping

	PEO 1	PEO 2	PEO 3	PEO 4
Mission Statement 1	3	3	2	2
Mission Statement 2	3	3	2	2
Mission Statement 3	3	2	3	2
Mission Statement 4	3	2	3	3
Mission Statement 5	3	3	3	2

Program Specific Outcomes (PSO)

- 1. Recognize, research, and resolve a wide range of practical issues in the field of VLSI.
- 2. Develop skills to build and create systems in the expanding fields of VLSI to solve the problems of the modern economy.
- 3. Demonstrate exemplary leadership attributes and actively pursue the advancement of many entities, including organizations, the environment, and society at large. by upholding their professional obligations with a strong commitment to ethical conduct.

Mapping Program Educational Objectives (PEO) to Program Learning Outcomes (PLO)

				Progra	am Learn	ing Outco	mes (PLC))							
	POs												PSOs		
PEOs	Engineering Knowledge	Design Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Lifelong Learning	PSO 1	PSO 2	PSO 3		
PEO 1	3	3	3	3	2	1	3	2	2	2	3	2	2		
PEO 2	3	3	3	3	3	1	3	1	2	2	3	2	3		
PEO 3	3	3	3	3	3	3	3	3	3	3	2	3	3		
PEO 4	2	3	2	2	2	3	3	1	2	2	3	3	3		

Category Wise Credit	Distribution		
Course Sub-Category	Sub-Category Credits	Category Credits	Learning Hours
Ability Enhancement Courses (AEC)		1	
University AEC	0		30
School AEC	1		
Value Added Courses (VAC)		1	
University VAC	1		30
School VAC	0		
Skill Enhancement Courses (SEC)		4	
School SEC	4		120
Department SEC	0		120
SEC Elective	0		
Foundation / Interdisciplinary courses (FIC)	R	3	
School FIC	0		90
Department FIC	3		
Core + Core Elective including Specialization (CC)	105 9 Martin	36	
Core	28		1080
Core Elective (Inc Specialization)	8		
Minor (MC) + Open Elective (OE)	0	0	0
Research / Design / Internship/ Project (RDIP)	1	35	
Internship / Design Project / Startup / NGO	3		1050
Internship / Research / Thesis	32		
	Total	80	2430

Semester wise Course Credit Distri	bution	Unde	r Vari	ous Ca	tegories	
C.A			S	emester		
Category	Ι	II	III	IV	Total	%
Ability Enhancement Courses - AEC	0	1	0	0	1	1
Value Added Courses - VAC	0	1	0	0	1	1
Skill Enhancement Courses - SEC	2	2	0	0	4	5
Foundation / Interdisciplinary Courses - FIC	3	0	0	0	3	4
CC / SE / CE / TE / DE / HSS	16	20	0	0	36	44
Minor / Open Elective - OE	0	0	0	0	0	0
(Research/ Design/ Industrial Practice/Project/Thesis/Internship) -RDIP	0	3	17	15	35	43
Grand Total	22	27	17	15	80	100

Note: L-T/D-P/Pr and the class allocation is as follows.

- a) Learning Hours : 30 learning hours are equal to 1 credit.
- b) Lecture/Tutorial : 15 contact hours (60 minutes each) per semester are equal to 1 credit.
- c) Discussion : 30 contact hours (60 minutes each) per semester are equal to 1 credit.
- d) Practical : 30 contact hours (60 minutes each) per semester are equal to 1 credit.
- e) Project : 30 project hours (60 minutes each) per semester are equal to 1 credit.

				SEMESTER - I				
S. No	Category	Sub- Category	Course Code	Course Title	L	T/D	P/Pr	С
1	VAC	U VAC	VAC 501	Community Engagement and Social Responsibility		0	1	1*
2	AEC	S AEC	AEC 502	Research Seminar - I	0	0	1	1*
3	SEC	S SEC	SEC 502	Design Thinking	1	0	1	2
4	FIC	D FIC	FIC 503	AI/ML Techniques	2	0	1	3
5	Core	CC	VLS 501	CMOS Digital IC Design	3	0	1	4
6	Core	CC	VLS 502	CMOS Analog and Mixed Signal IC Design	3	0	1	4
7	Core	CC	VLS 503	VLSI Technology	3	1	0	4
8	Core	CC	VLS 504	VLSI Physical Design	3	0	1	4
			S.	Semester Total	15	1	7	22
		- d*	1	1 4 4 7 1 4 7 4 7 4 7 4 7 4 1 7 4 1 7 4 1 7 4 1 7 4 1 7 4 1 7 4 1 7 4 1 7 4 1 7 4 1 7 4 1 7 4 1 7 4 1 7 4 1 7 4				

				SEMESTER - II				
S. No	Category	Sub- Category	Course Code	SEMESTER - IIurse odeCourse TitleLT/DI2 502Community Engagement and Social Responsibility002 503Research Seminar - II002 103Entrepreneurial mindset102 EIndustry - Core Elective2 EIndustry - Core Elective3 505VLSI Testing and Verification303 506Semiconductor Device Modelling303 507Advanced HDL based FPGA Design30		P/Pr	С	
1	VAC	U VAC	VAC 502	Community Engagement and Social Responsibility	0	0	1	1
2	AEC	S AEC	AEC 503	Research Seminar - II	0	0	1	1
3	SEC	S SEC	SEC 103	Entrepreneurial mindset	1	0	1	2
4	Elective	CE	CE	Industry - Core Elective				4
5	Elective	CE	CE	Industry - Core Elective				4
6	Core	CC	VLS 505	VLSI Testing and Verification	3	0	1	4
7	Core	CC	VLS 506	Semiconductor Device Modelling	3	0	1	4
8	Core	CC	VLS 507	Advanced HDL based FPGA Design	3	0	1	4
9	RDIP	RDIP	VLS 508	Project Management	0	0	3	3
				Semester Total	16	2	9	27

	SEMESTER - III										
S. No	Category	Sub- Category	Course Code	Course Title	L	T/D	P/Pr	С			
1	RDIP	RDIP	VLS 509	Thesis - I	0	0	14	14			
2	RDIP	RDIP	VLS 510	Industrial Practice	0	0	3	3			
				Semester Total	0	0	17	17			

	SEMESTER - IV										
S. No	Category	Sub- Category	Course Code	Course Title	L	T/D	P/Pr	С			
1	RDIP	RDIP	VLS 511	Thesis - II	0	0	15	15			
				Semester Total	0	0	15	15			
	S TO B A										

			Li	st of Core Electives				
S. No	Category	Sub- Category	Course Code	Course Title	L	T/D	P/Pr	С
1	CE	CE	VLS 533	Embedded Programming	3	1	0	4
2	CE	CE	VLS 535	Hardware Accelerators for IoT Edge Computing	3	0	1	4
3	CE	CE	VLS 562	Sensor Technology and MEMS	3	1	0	4
4	CE	CE	VLS 530	CAD for VLSI	3	0	1	4
5	CE	CE	VLS 555	More than Moore's electronics	3	1	0	4



Research Seminar

Course Code	AEC 502	Course Category AEC				Ĺ	Т	Р	С
Course Code	AEC 302	Course Category	AEC			0	0	1	1
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)					
Course Offering Department	ECE	Professional / Licensing Standards							

Course Objectives / Course Learning Rationales (CLRs)

- 1. Survey the existing research works/literature and analyse them.
- 2. Attain adequate knowledge of a research problem chosen.
- 3. Improve the presentation/communication skills to articulate their research work.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Review and analyse the existing research work in a systematic way.	3	80%	70%
Outcome 2	Attain strong technical, domain knowledge in the research topic chosen.	3	80%	70%
Outcome 3	Attain good presentation skills to articulate the research problem, analysis and its solution	2	80%	70%

					Pro	ogram L	earning	Outcom	es (PLO))			
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	1 OSA	PSO 2	PSO 3
Outcome 1	3	2	2				2	2	2	1	3	3	2
Outcome 2	3	2	3				2	1	2	1	3	3	3
Outcome 3	1	1	1			1	2	1	2	1	3	1	1
Average	2	2	3			1	2	2	2	1	3	2	3

Student is expected to spend minimum 2 hours/week for the Project work.

Learning Assessment

		Contin	uous Learning	Assessmei	nts (50%)	End Seme	ster Exam (50%)	
Bloom's Lev	el of Cognitive Task	Review -I		Mid Rev	view	Final Review		
		Th	Prac	Th	Prac	Th	Prac	
Laval 1	Remember		200/		200/		200/	
Level I	Understand		20%		2070		20%	
Lovel 2	Apply		800/		8004		8004	
Level 2	Analyse		8070		8070		8070	
Laval 2	Evaluate							
Level 5	Create							
	Total		100%		100%		100%	

Recommended Resources

1.

Other Resources

1.

Course Designers

1. Dr. Rituparna Chowdhury, Assistant Professor, Dept. of ECE. SRM University - AP



Design Thinking

Course Code	SEC 502	Course Cotogomy	SEC		L	Т	Р	С
Course Coue	SEC 302	Course Calegory	SEC		1	0	1	2
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	Management	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. Familiarize with the principles of Design Thinking
- 2. Learn to apply the principles of Design Thinking
- 3. Apply Design Thinking to solve problems.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Grasp the Concepts and process of Design Thinking	2	85%	90%
Outcome 2	Learn the process of Design Thinking	2	85%	90%
Outcome 3	Solve a problem using Design Thinking Principles	5	75%	65%

					Progra	am Lea	rning O	utcome	s (PLO)					
					Р	Os					PSOs			
PEOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tool Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork	Communication	Life-long Learning	PSO 1	PSO 2	PSO 3	
Outcome 1	3									1	3	1	3	
Outcome 2	3							3		2	3	2	3	
Outcome 3	3	3	3	3				3	3	3	3	3	3	
Average	3	3	3	3				3	3	2	3	2	3	

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	Incubation and understanding			1,2
	Understanding of Design Thinking & its Importance	4	1	1,2
	Importance of Design Thinking	3	1	1,2
	Pillars of Design Thinking	3	1	1,2
Unit 2	Process – Understanding the Stages of Design Thinking			1,2
	Stage 1- Empathy	2	2	1,2
	Stage 2 - Define	2		
	Stage 3 – Ideate	2		
	Stage 4 – Prototype	2	2	1,2
	Stage 5 – Test & Implement	2	2	1,2
Unit 3	Application			
	Project Work	7	3	1,2
	Viva	3	3	1,2
	Total Contact Hours		30	•

Learning Assessment

Dloom?	Lovel of Cognitive Tesl	Continuous Learning	Assessments (100%)
DIOOIII	Level of Cognitive Task	CLA-1 (50%)	CLA-2 (50%)
L aval 1	Remember	20	40
Level I	Understand	20	40
Level 2	Apply	30	30
Level 2	Analyse		30
Level 2	Evaluate	50	30
Level 5	Create	50	30
	Total	100%	100%

Recommended Resources

1. Design Thinking - Techniques and Approaches, N. Siva Prasad

Other Resources

- 1. HBS Online Design Thinking & Innovation course material
- 2. Case studies
- 3. Nigel Cross, Design Thinking, BERG Publishing, (2011)
- 4. Thomas Lockwood, Design Thinking- Integrating Innovation, Customer Experience and Brand Value, , Design Management Institute, (2009)

Course Designers

1. Satyanarayana Duvvuri, Visiting Faculty, Paari school of business, SRM University AP.



AI/ML Techniques

Course Code	EIC 502	Course Cotogom	EIC		Ι	Т	Р	С
Course Code	FIC 303	Course Category	ГЮ		2	0	1	3
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. To familiarize the domains of supervised and unsupervised learning.
- 2. To understand and apply various binary classifiers.
- 3. To understand and apply clustering methods.
- 4. To understand and analyze Feedforward neural networks and CNNs
- 5. Able to work on real time projects related to AI/ML

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Familiarize supervised and unsupervised learning	1	85%	80%
Outcome 2	Understand and Apply various binary classifiers	1, 2	80%	75%
Outcome 3	Understand and Apply clustering methods	1, 2	85%	70%
Outcome 4	Understand and Evaluate Feedforward neural networks	3	80%	70%
Outcome 5	Understand the CNNs and able to work on real time projects	2,3,4	75%	70%

					Pr	ogram L	earning	Outcom	es (PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	1	1	1	1	1						1	1	1
Outcome 2	2	3	2	3	2				2	1	1	2	3
Outcome 3	2	2	2	3	3				2	1	1	2	2
Outcome 4	2	3	3	3	3				2	1	2	3	3
Outcome 5	3	3	2	3	3				2	1	2	2	2
Average	2	3	2	3	3				2	1	1	2	2

Unit	Unit Name	Required Contact	CLOs	References
No.		Hours	Addressed	Used
Unit 1	Introduction	6		
	Introduction to machine learning	1	1	1, 2,3
	Supervised learning	1	1	1, 2,3
	Unsupervised learning	1	1	1, 2,3
	Linear regression	2	1	1, 2,3
	Logistic regression	1	1	1, 2,3
Unit 2	Classifiers	7		
	Naive Bayes	1	2	1, 2,3
	Support Vector Machines	2	2	1, 2,3
	K-Nearest Neighbor	1	2	1, 2,3
	Decision Trees	2	2	1, 2,3
	Random forest	1	2	1, 2,3
Unit 3	Clustering	6		
	Clustering in machine learning	1	3	1, 2,3
	Different types of clustering algorithms	1	3	1, 2,3
	K-Means clustering	2	3	1, 2,3
	Loss functions in regression and classification	1	3	1, 2,3
	Bias-variance trade off	1	3	1, 2,3
Unit 4	Feedforward neural networks	7		
	Introduction to Neural Networks	1	4	1, 2,3
	Activation functions	1	4	1,2,3
	Feed-forward Network	2	4	1, 2,3
	Backpropagation algorithm	2	4	1, 2,3
	Introduction to convolutional neural network (CNN)	1	5	1, 2,3
Unit 5	Applications of AI/ML	6		
	Applications in VLSI	3	5	4
	Applications in IoT	3	5	4
	Total Contact Hours	45	1	1

Learning Assessment

		Conti	nuous l	earnin	g Asses	ssment	:s (50%)			End Semest	ter Exam
Bloom's L	evel of Cognitive.	CLA-1		Mi	d-1	CL	CLA-2		A-3	(50%)	
	Task		0%)	(15%)		(10%)		(15%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Lovel 1	Remember	4006	4006	6004	400%	4006	4006	6004	4006	2004	4004
Level	Understand	40%	40 %	0070	40%	4070	4070	0070	4070	30%	40%
	Apply	60%	60%	400%	60%	60%	60%	400%	60%	70%	60%
Level Z	Analyse	00%	00%	40%	00%	00%	00%	4070	00%	70%	0070
	Evaluate										
Levels	Create										
Total		100%		100%	•	100%		100%		100%	

Recommended Resources

- 1. Christopher M. Bishop, "Pattern Recognition and Machine Learning" by Springer, 2007.
- 2. Tom M. Mitchell, "Machine Learning", First Edition by Tata McGraw-Hill Education, 2013.
- 3. Luis G. Serrano, "Grooking Machine Learning" 2nd Edition, Manning Publications, 2021.
- 4. Reference papers from various journals such as IEEE, Elsevier etc.

Other Resources

Course Designers

1. Dr. Sudhakar Tummala. Asst. Professor. And Dr. V. Udaya Sankar, Asst. Professor, Dept. Of ECE. SRM University - AP



CMOS Digital IC Design

Course Code	VI S 501	Course Cotogowy	CC		L	Т	Р	С
Course Code	VLS 301	Course Category	CC .		3	0	1	4
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. To understand the fundamental principles of CMOS technology, including the operation of MOS transistors, logic gates, and basic building blocks.
- 2. To learn the techniques for designing and analyzing CMOS digital circuits, including combinational and sequential logic circuits.
- 3. To gain proficiency in creating layout designs for CMOS circuits (considering area, power, and performance) and understand the importance of timing in digital circuits, and learn how to perform timing analysis for CMOS circuits.
- 4. To apply the knowledge gained in the course through hands-on projects that involve the design, simulation, and layout of CMOS digital circuits.

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the fundamental principles of CMOS Technology along with its advantages and limitations	2	85%	80%
Outcome 2	Design both combinational & sequential circuits using CMOS technology	3	80%	75%
Outcome 3	Create layout designs for CMOS digital circuits and understand the impact of the fabrication process on circuit design	3	85%	70%
Outcome 4	Apply theoretical knowledge to real-world digital IC design projects	3	80%	70%

Course Outcomes / Course Learning Outcomes (CLOs)

					Pr	ogram L	earning	Outcom	es (PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	£ OSA
Outcome 1	3	2	2	2	2	3	2	2	2	3	2	3	2
Outcome 2	3	3	3	2	2	1	2	2	3	3	2	3	3
Outcome 3	3	3	3	3	2	1	2	2	3	2	2	3	3
Outcome 4	3	3	3	3	2	3	3	3	3	3	3	3	3
Average	3	3	3	2	2	2	2	2	3	3	2	3	3

Unit	Unit Name	Required	CLOs	References
NO.	MOSEET Introduction and Layout of CMOS Logic Circuits	Contact Hours	Addressed	
Unit I		y		1.2
1.	Basic MOSFET Characteristics– Threshold Voltage, Body Bias concept, Current- Voltage Characteristics – Square-Law Model	2	1	1,2
2.	MOSFET Modeling– Drain-Source Resistance, MOSFET Capacitances	1	1	1,2
3.	Geometric Scaling Theory– Full-Voltage Scaling, Constant-Voltage Scaling, Challenges of MOSFET Scaling	2	1	1,2
4.	CMOS fabrication processing steps	1	1	1,2,4,6
5.	Design Rules, Stick diagram, Layout of logic circuits	2	1,3	
6.	Layout of logic circuits, latch-up	1	1,3	1,2,4,6
Unit 2	Switching Properties of MOSFET and CMOS Inverter	8		
7.	Static and dynamic characteristics of Pass Transistors	1	1,2	1,2
8.	Transmission Gate, TG based logic circuits, Introduction to CMOS Inverter	2	1,2	1,2
9.	CMOS Inverter - DC Characteristics, Noise Margins, Layout Considerations	1	1,2	1,2
10.	Inverter Switching Characteristics, Transient Effects on the VTC, RC Delay Modeling, Elmore Delay, Output Capacitance	2	1,2	1,2
11.	Inverter Design – DC Design, Transient Design, Driving Large Capacitive Loads	2	1,2	1,2
Unit 3	Static CMOS Logic Elements & Power Dissipation in CMOS Logic Circuits	9		
12.	CMOS NAND Gate, CMOS NOR Gate	1	2,3	1,2,3
13.	CMOS AND, OR, NOT, and Complex Logic Functions	2	2,3	1,2,3
14.	CMOS SRAM and DRAM Cell	1	2,3	1,2,3
15.	Dynamic Power Dissipation-Switching Power Dissipation	2	2,3	1,2,3
16.	Short Circuit Power Dissipation, Glitching Power Dissipation	1	1,3	1,2,3
17.	Static Power Dissipation, Diode Leakage Current, Subthreshold Leakage Current	2	1,3	1,2,3
Unit 4	Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families	9		
18.	Charge Leakage in CMOS circuits	2	2,4	1,2,5
19.	Charge Sharing, Dynamic RAM Cell	2	2,4	1,2,5
20.	Clocked-CMOS	2	2,4	1,2,5
21.	Pre-Charge/ Evaluate Logic, Domino Logic	2	2,4	1,2,5
	CMOS Single-Phase Logic	1	2,4	1,2,5
Unit 5	Issues In Chip Design	8		
22.	ESD Protection	2	2,3,4	1,2,5
23.	On-Chip Interconnects – Line Parasitics	1	2,3,4	1,2,5
24.	Modeling of the Interconnect Line	2	2,3,4	1,2,5
25.	Clock Distribution	2	2,3,4	1,2,5
26.	Input-Output circuits	1	2,3,4	1,2,5
	Total		43	

Exp No.	Experiment Name	Required Contact Hours	CLOs Addressed	References Used
	Lab Experiment / Practical / Programming 1			
	Lab Experiment / Practical / Programming 2			
	Lab Experiment / Practical / Programming 3			
	Lab Experiment / Practical / Programming 4			
	Lab Experiment / Practical / Programming 5			
	Lab Experiment / Practical / Programming 6			
Total C	ontact Hours			

Learning Assessment Theory

Bloom's Level of Cognitive Task		Cont	inuous Learnii	ng Assessments ((50%)	End Semester Exam	
		CLA-1 (10%)	Mid-1 (15%)	CLA-2 (15%)	CLA-3 (10%)	(50%)	
Level 1	Remember	40%	60%		50%	30%	
	Understand	4070	0070		5070	5070	
Level 2	Apply	60%	40%	20%	50%	60%	
Level 2	Analyse	0070	4070	2070	5070	0070	
Loval 2	Evaluate			800/		100/	
Level 5	Create			00%		1070	
Total		100%	100%	100%	100%	100%	

Learning Assessment (Lab)

Bloom	n's Level of	Contin	Continuous Learning Assessments (50%)						
Cognitive Task		Experiments (20%)	Record / Observation Note (10%)	Viva + Model (20%)	- (50%)				
Level 1	Remember	40%	60%	50%	40%				
	Understand	4070	0070	5070					
Level 2	Apply	40%	40%	40%	40%				
Level 2	Analyse	40%	40 / 0	40 /0					
Lovel 3	Evaluate	2004	10%	100/	20%				
Level 5	Create	2070	1078	10 /0					
Total		100%	100%	100%	100%				

Recommended Resources

- 1. Rabaey, J.M., Chandrakasen, A.P. and Nikolic, B., Digital Integrated Circuits A Design perspective, Pearson Education (2007) 2nd ed.
- 2. Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits Analysis and Design, Tata McGraw Hill
- 3. J P Uyemura, CMOS Circuit Design, Springer
- 4. Weste, N.H.E. and Eshraghian, K., CMOS VLSI Design: A Circuits and Systems Perspective, eddision Wesley (1998) 2nd ed.
- 5. Baker, R.J., Lee, H. W. and Boyce, D. E., CMOS Circuit Design, Layout and Simulation, Wiley IEEE Press (2004) 2nd ed.
- 6. Weste, N.H.E., Harris, D. and Banerjee, A., CMOS VLSI Design, Dorling Kindersley (2006) 3rd ed.

Other Resources

1. James D. Plummer, Michael D. Deal, Peter B. Griffin, Silicon VLSI Technology: Fundamentals, Practice and Modeling, Pearson Education, 2009.

Course Designers

1. Dr. M. Durga Prakash, Asst. Professor. Dept. of ECE. SRM University - AP.



CMOS Analog and Mixed Signal IC Design

Course Code	VI S 502 Course Category CC			Ι		Т	Р	С	
Course Code	VLS 302	Course Category	ourse Category CC			;	0	1	4
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)					
Course Offering Department	ECE	Professional / Licensing Standards							

Course Objectives / Course Learning Rationales (CLRs)

- 1. To understand the fundamentals of Analog IC Design, including the single-stage amplifiers and Differential Amplifiers
- 2. To learn the general considerations for Operational Amplifiers designing and performance of various Op-Amp topologies
- 3. To understand the stability in feedback systems and noise in mixed signal IC design
- 4. To apply the data converters knowledge gained in the course through hands-on projects that involve the design, simulation, and layout of CMOS analog circuits.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the fundamental of analog IC Design, including the single-stage amplifiers and Differential Amplifiers	2	85%	80%
Outcome 2	Design operational amplifiers and performance of various Op-Amp topologies	3	80%	75%
Outcome 3	Create layout designs for operational amplifier circuits and understand the stability in feedback system and noise performance	3	85%	70%
Outcome 4	Apply theoretical knowledge to real-world analog and digital converter IC design projects	3	80%	70%

					Prog	gram Lea	arning O	utcomes	(PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	2 OSA	£ OSA
Outcome 1	3	2	2	2	3	2	2	2	3	2	2	3	2
Outcome 2	3	3	3	2	1	2	2	3	3	3	2	3	3
Outcome 3	3	3	3	2	1	2	2	3	2	3	2	3	3
Outcome 4	3	3	3	2	3	3	3	3	3	3	3	3	3
Average	3	3	3	2	2	2	2	3	3	3	2	3	3

Course Unitization Plan Theory

Unit	Unit Nama	Required	CLOs	Rafarancas
No.	Unit Name	Contact Hours	Addressed	Kelefences
Unit 1	Introduction to Analog Integrated Design	10		
1.	Models for analog design, body transconductance, Single-stage	2	1	1,2
	Amplifiers - CS stage, diode connected load	2	1	
2.	Current source load and source degeneration Review of CD and CG	2	1	1,2
	stages	2	1	
3.	Cascode stage & folded Cascode concepts	1	1	1,2
4.	Design of amplifier from specifications Differential Amplifiers	1	1	1,2,4
5.	MOS differential pair, Small signal operation. half circuit analysis	2	1.2	
	common mode response	2	1,5	
6.	Differential amplifier with active load, common mode gain, and	2	1.2	1,2,4
	CMRR. Frequency response of the differential amplifier.	2	1,5	
Unit 2	Operational Amplifiers	10		
7.	General considerations – performance parameters	1	1,2	1,2
8.	One-Stage Op amps – Cascode Op-Amps Telescopic Op-Amps	2	1,2	1,2
9.	Folded Cascode Op-Amps	1	1,2	1,2
10.	Two-Stage Op amps, Gain boosting	1	1,2	1,2
11.	Comparison of performance of various Op-Amp topologies	2	1,2	1,2
12.	Design of Op-Amps from specifications.	2	1,2	1,2
13.	Review of bode rules	1	1,2	1,2
Unit 3	Stability In Feedback Systems	9	1,2	1,2
15.	Problem of instability, Stability condition	1	2,3	1,2,3
16.	Gain-phase crossovers, phase margin	2	2,3	1,2,3
17.	Frequency compensation: frequency response of cs amplifier,	1	2,3	1,2,3
	Miller effect			
18.	Poles in a system, Pole-splitting, miller compensation	2	2,3	1,2,3
19.	Two-stage Op-Amp - compensation techniques	1	1,3	1,2,3
20.	Closed-loop stability, optimal phase margin.	2	1,3	1,2,3
Unit 4	Noise	9		
21.	MOSFET noise models, types of noise, thermal noise, flicker noise	2	2,4	1,2,5
22.	Representation of noise in circuits, Noise in single-stage amplifiers	2	2,4	1,2,5
23.	Integrated Oscillators: Ring oscillators	2	2,4	1,2,5
24.	LC oscillators - Cross coupled oscillators, VCO.	2	2,4	1,2,5
Unit 5	Data Converters	7		
25.	DAC and ADC Specifications, Current Steering DAC	2	2,3,4	1,2,5
26.	Charge Scaling DAC, Cyclic DAC	2	2,3,4	1,2,5
27.	Pipeline DAC, Flash ADC	2	2,3,4	1,2,5
28.	Pipeline ADC, Integrating ADC, Successive Approximation ADC.	2	2,3,4	1,2,5
	Total Hours		45	

Course Unitization Plan - Lab

Exp No.	Experiment Name	Required Contact Hours	CLOs Addressed	References Used
1	 Design an Inverter with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) Transient Analysis b. Draw the Layout and verify the DRC, ERC c. Extract RC and back annotate the same and verify the Design d. Verify & Optimize for Time, Power and Area to the given constraint. 	2	2,3	1,2,3
2	Design the following circuits with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS.	2	3	1,2,3
3	Single stage amplifier	2	3	1,2,3
4	Comparator.	2	2,3	1,2,3
5	Differential amplifier	2	3	1,2,3
6	Operational Amplifier	2	3	1,2,3
7	Ring Oscillator	2	2,3	1,2,3
8	VCO	2	1,2	1,2,3
9	Digital to Analog Converter	2	2,3	1,2,3
10	Analog to Digital Converter	2	2,3	1,2,3
	Total Contact Hours		20	

Learning Assessment Theory

Bloom's Level of Cognitive Task			End Semester			
		CLA-1 (10%)	CLA-1 (10%) Mid-1 (15%) CLA-2 (15%) CI		CLA-3 (10%)	Exam (50%)
Loyal 1	Remember	40%	60%		50%	30%
Level I	Understand	4070	0070			5070
L aval 2	Apply	60%	40%	20%	50%	60%
Level 2	Analyse	0070	4070	2070	5070	0070
Level 3	Evaluate			8004		1.09/
	Create			8070		1070
Total		100%	100%	100%	100%	100%

Learning Assessment (Lab)

Bloor	n's Loval of	Conti	End Semester Exam		
Cognitive Task		Experiments (20%)	Record / Observation Note (10%)	Viva + Model (20%)	(50%)
L and 1	Remember	400/	<u>(0)</u>	500/	40%
Level I	Understand	40%	00%	30%	
Loval 2	Apply	40%	40%	40%	40%
	Analyse	4070	+070	4070	
Lovol 3	Evaluate	20%	10%	10%	20%
Level 5	Create	2070	1070	1070	
Total		100%	100%	100%	100%

Recommended Resources

- 1. Design of Analog CMOS Integrated Circuits, Behzad Razavi, 2002, Mc GrawHill Edition, ISBN: 0-07-238032-2.
- 2. CMOS Circuit Design, Layout and Simulation, R. Jacob Baker, Harry W. Li and David E. Boyce, 2002, IEEE Press, ISBN: 81-203-1682-7.
- 3. CMOS Mixed-signal Circuit Design, R. Jacob Baker, 2009, IEEE Press, ISBN: 978-81-265-1657-5.
- Analysis and Design of Analog Integrated Circuits, Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "", 4th edition, 2008, Wiley India Private Limited, ISBN:978-8126515691.
- 5. Fundamentals of Microelectronics, Behzad Razavi, 2nd Edition, 2013, Wiley, ISBN- 10: 1118156323

Other Resources

Course Designers

1. Dr. M. Durga Prakash. Asst. Professor. Dept. Of ECE. SRM University - AP



VLSI Technology

Course Code	VI S 502	Course Cotogowy	CC				Т	Р	С
Course Code	VLS 505	Course Calegory	CC .		3	1	0	4	
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)					
Course Offering Department	ECE	Professional / Licensing Standards							

Course Objectives / Course Learning Rationales (CLRs)

- 1. To study the various processes of IC fabrication.
- 2. To study the device fabrication process.
- 3. To understand various issues of defects and stresses in the films.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Outline the basics of semiconductor crystal properties	2	80%	75%
Outcome 2	Identify the fundamentals of IC fabrication	3	80%	75%
Outcome 3	Illustrate the different methods involved in VLSI fabrication process.	4	80%	75%
Outcome 4	Appreciate the advanced methods involved in IC fabrication.	4	80%	75%
Outcome 5	Build the knowledge of process integration-of devices	4	80%	75%
Outcome 6	Build the knowledge of Packaged the devices	4	80%	75%

					Progr	am Leai	ning Ou	itcomes ((PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	1	1	2	2	2	2	2	2	2	2	3	1
Outcome 2	3	1	1	2	2	2	2	2	2	2	2	3	1
Outcome 3	2	3	3	3	3	3	2	3	2	3	3	2	3
Outcome 4	2	3	3	3	3	3	3	3	1	3	3	2	3
Outcome 5	2	3	3	3	3	3	3	3	2	3	3	2	3
Outcome 6	2	3	3	3	3	3	3	3	1	3	3	2	3
Average	2	3	3	3	3	3	2	3	2	3	3	2	3

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References
Unit 1	Clean Room Environment and Wafer Preparation	10		
1	Crystal Structure of a solid	1	1	1,2
2	Defects in materials	1	1	1,2
3	Types of clean room, Contamination in clean room	2	1,2	1,2
4	Electronic Grade Silicon, Czochralski crystal growing	2	1,2	1,2,4,6
5	Silicon Shaping	2	1,2	
6	Wafer cleaning processes and wet chemical etching techniques	2	1,2	1,2,4,6
Unit 2	Oxidation, Diffusion, and Implantation	12		
7	Kinetics of Silicon dioxide growth both for thick, thin, and ultrathin films	3	2,3	1,2
8	Oxidation Techniques and Systems Models of Diffusion in Solids	2	2,3	1,2
9	Defects due to oxidation	2	1,2,3	1,2
10	Solid State diffusion modelling and technology	2	1,2,3	1,2
11	Implantation Equipment, Principles, techniques and applications	2	2,3	1,2
12	Removal of implant damage	1	2,3	
Unit 3	Epitaxial Growth, Metallization	12		
13	CVD and MBE	3	2,3	1,2,3
14	Defects in Epitaxial Layer Dielectric Deposition	2	2,3	1,2,3
15	PECVD and Rapid Thermal Annealing	2	2,3,4	1,2,3
17	E-beam evaporation	2	2,3,4	1,2,3
18	Sputtering and Thermal Evaporation	2	2,3	1,2,3
19	Etching	1	2,3,4	1,2,3
Unit 4	Lithography	6		
20	Optical Lithography	2	2,3,4	1,2,5
21	E-beam lithography	2	2,3,4	1,2,5
22	X-ray	1	2,3,4	1,2,5
23	Other Lithography techniques	1	2,3,4	1,2,5
Unit 5	Fabrication and Packaging	5		
24	Fabrication of MOSFET	2	3,4,5	1,2,5
25	Process to Package a chip (Dicing, Attaching, wire bonding, Chip package header)	2	2,3,4	1,2,5
26	Fabrications of other devices	1	2,3,4	1,2,5
	Total		45	

Learning Assessment

Bloom's L	evel of	0	End Semester			
Cognitive Task		CLA-1 (15%)	(15%) Mid-1 (15%) CLA-2 (10%)		CLA-3 (10%)	Exam (50%)
Lavel 1.2	Understand	40%	40%	20%	30%	30%
Level 1,2	Apply	-1070	4070		5070	5070
	Understand 40% 40% 30%		30%	50%		
Level 2,3	Apply	4070	4070	4070	5070	5070
T1 2 4	Apply	20%	20%	409/	40%	20%
Analyse			4070		2070	
,	Total	100%	100%	100%	100%	100%

Recommended Resources

- 1. S.M. Sze, "VLSI Technology", McGraw Hill, 2nd Edition. 2008
- 2. G. S. May, S. M. Sze, "Fundamentals of Semiconductor Fabrication" Wiley, 2003
- 3. James D Plummer, Michael D. Deal, Peter Griffin, "Silicon VLSI Technology: fundamentals practice and Modeling", Prentice Hall India, 2009.
- 4. Wai Kai Chen, "VLSI Technology" CRC press, 2003.
- 5. S.K. Gandhi, VLSI Fabrication principles, Wiley.

Other Resources

Course Designers

1. Dr. Manas Ranjan Tripathy. Asst. Professor. Dept. Of ECE. SRM University - AP



VLSI Physical Design

Course Code	VI S 504	Course Cotogomy	CC	L	Т	Р	С	
Course Coue	VLS 304	Course Category CC			3	0	1	4
Pre-Requisite Course(s)	VLSI Design	Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. To understand the requirements of VLSI automation Tools.
- 2. To understand the requirements Proper placement and Routing of Circuits.
- 3. To familiarize with methods and algorithms for efficient Floor Planning and Routing
- 4. To understand different circuit level techniques for logic synthesis.
- 5. To understand how high-level synthesis is carried out for proper allocation, scheduling and assignment.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Describe various VLSI Automation Tools	2	70%	65%
Outcome 2	Implement ideas on Placement and Partitioning of Circuits	3	70%	65%
Outcome 3	Identify concepts and Algorithms of Floor planning and Routing	3	70%	65%
Outcome 4	Develop circuit level techniques and apply in logic Synthesis	3	70%	65%
Outcome 5	Working on High Level Synthesis of Circuits	4	70%	65%

					Prog	gram Lea	arning O	utcomes	(PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	1 OSA	2 OS4	PSO 3
Outcome 1	3	3	3	1		2					3	1	2
Outcome 2	3	3	3	2	1	2		3			3	2	2
Outcome 3	3	3	3	2		2		3			3	2	2
Outcome 4	3	3	3	2	1	2		3			3	2	2
Outcome 5	3	3	3	2	1	2		2			3	2	2
Average	3	3	3	1	1	2		3			3	2	2

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	VLSI DESIGN AUTOMATION TOOLS	10		
	Algorithms and system design, Structural and logic design	2	1	1
	Transistor level design, Layout design	2	1	1
	Verification methods	1	1	1
	Design management tools	1	1	1
	To verify and simulation of 4 bit adder by using INCISIVE tool. (Lab Experiment - 1)	2	1	4
	To verify and simulation of 4 bit counter by using INCISIVE tool. (Lab Experiment - 2)	2	1	4
Unit 2	PHYSICAL DESIGN OVERVIEW	14		
	Layout compaction	2	2	1
	placement and routing, Pin Assignment	2	2	1
	Design rules, symbolic layout, Applications of compaction	2	2	2
	Formulation methods, Algorithms for constrained graph compaction	2	2	2
	Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms	2	2	2
	To verify and simulation of 4 bit adder by using INCISIVE tool. (Lab Experiment - 1)	2	1	4
	To verify and simulation of 4 bit counter by using INCISIVE tool. (Lab Experiment - 2)	2	1	4
Unit 3	FLOOR PLANNING AND ROUTING	10		
	Floor planning concepts	2	3	1,2
	Shape functions and floor planning sizing	2	3	1,2
	Local routing, Area routing	2	3	1,2
	Channel routing	2	3	1,2
	Global routing and its algorithms.	2	3	1,2
	To import design & floor planning of 16-bit adder using INNOVUS tool in cadence. (Lab Experiment - 5)	2	3	5
	To import design & floor planning of 16-bit counter using INNOVUS tool in cadence (Lab Experiment - 6)	2	3	5
	To design power planning of 8-bit adder in cadence. (Lab Experiment - 7)	2	3	5
Unit 4	SIMULATION AND LOGIC SYNTHESIS	10		
	Gate level and switch level modelling and simulation	1	4	2,3
	Introduction to combinational logic synthesis	1	4	2,3
	STA	2	4	2,3

	ROBDD principles, Implementation, construction and manipulation	2	4	2,3
	Two level logic synthesis.	2	4	3,4
	Timing Closure	2	4	3,4
	To design power planning of 16-bit counter in cadence. (Lab Experiment - 8)	2	4	4
Unit 5	HIGH-LEVEL SYNTHESIS	11		
	Hardware model for high level synthesis	2	5	3,4
	Internal representation of input algorithms	1	5	3,4
	Allocation, assignment, and scheduling	2	5	3,4
	Scheduling algorithms, Aspects of assignment	1	5	3,4
	High level transformations	1	5	3,4
	To design placement, routing & GDS of 8-bit adder in cadence. (Lab Experiment - 9)	2	5	4
	To design placement, routing & GDS of 16-bit counter in cadence. (Lab Experiment - 10)	2	5	4
	Total		47	

Learning Assessment

Bloom's Level of Cognitive Task			Cor	ntinuous	Learnin	g Assessi	ments (6)%)		End Semester Exam		
		CLA-1 (15%)		Mid-1	Mid-1 (15%)		CLA-2 (15%)		(15%)	(40%)		
		Th	Par	Th	Par	Th	Par	Th	Par	Th	Par	
Loval 1	Remember	60%	2004	50%	409/	60%	2004	50%	409/	400/	50%	
Level I	Understand	0070	5070	5070	4070	0070	3070	3076	4070	4070	3070	
Lavel 2	Apply	400/	50%	50%	50%	409/	60%	50%	50%	600/	409/	
Level 2	Analyze	4070		3070		4070	0070	3070	30%	0070	4070	
Laval 2	Evaluate		2004		109/		1.09/		1.09/		1.00/	
Create			2070		1070		1070		1070		1070	
Total		100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	

Recommended Resources

- 1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley ,1998.
- 2. N.A.Sherwani, "Algorithms for VLSI Physical Design Automation", (3/e), Kluwer, 1999..
- 3. S.M. Sait, H. Youssef, "VLSI Physical Design Automation", World scientific, 1999

Other Resources

Course Designers

1. Dr. Ramesh Vaddi, Associate Professor, Dept of ECE, SRM University - AP



COMMUNITY SERVICE AND SOCIAL RESPONSIBILITY

Course Code	VAC 502	Course Cotogowy	VAC		L	Т	Р	С
Course Code	VAC 502	Course Calegory	VAC		0	0	2	2
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	CEL	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. Encourage initiatives that address local needs, foster self-sufficiency, and promote environmental sustainability within the community.
- 2. Equip participants with a deeper understanding of social issues and a sense of responsibility towards marginalized communities.
- 3. Inspire active participation in community service programs and foster a culture of giving back among individuals and organizations.
- 4. Develop and implement programs that contribute to skill development, economic empowerment, and equal opportunities for underprivileged sections of society.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Develop effective strategies for identifying and addressing community needs.	3	80%	80%
Outcome 2	Demonstrate empathy and cultural sensitivity when engaging with diverse community groups.	4	80%	75%
Outcome 3	Implement sustainable solutions and evaluate their impact on social well-being.	5	90%	85%
Outcome 4	Collaborate effectively within teams to design and lead community service projects.	6	90%	80%

Learning Assessment

Bloom's Level of Cognitive Task		C	End Semester			
		CLA-1 20%	CLA-1 20% Mid-1 20% CLA-2 20% CLA-3 20%		CLA-3 20%	Exam 50%
Level 1	Remember	10%	10%			20%
	Understand	1070	1070			2070
Level 2	Apply	-	10%	10%		20%
	Analyse		1070	1070		2070
Level 3	Evaluate	-			10%	10%
Levers	Level 3 Create				1070	1070
Total		10%	20%	10%	10%	50%



Research Seminar- II

Course Code	AEC 502	Course Cotogowy	AEC		L	Т	Р	С
Course Code	AEC 505	Course Category	AEC		0	0	1	1
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department		Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. Survey the existing research works/literature and analyse them.
- 2. Attain adequate knowledge of a research problem chosen.
- 3. Improve the presentation/communication skills to articulate their research work.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Review and analyse the existing research work in a systematic way.	3	80%	70%
Outcome 2	Attain strong technical, domain knowledge in the research topic chosen.	3	80%	70%
Outcome 3	Attain good presentation skills to articulate the research problem, analysis and its solution	2	80%	70%

					Prog	gram Lea	arning O	utcomes	(PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2				2	2	2	1	3	3	2
Outcome 2	3	2	3				2	1	2	1	3	3	3
Outcome 3	1	1	1			1	2	1	2	1	3	1	1
Average	2	2	3			1	2	2	2	1	3	2	3

Unit	Unit Name	Required	CLOs	References
No.		Contact Hours	Addressed	Used
Unit 1				
Unit 2				
Unit 3				
Unit 4				
Unit 5				

Learning Assessment

Bloom's Level of Cognitive Task		Contin	uous Learning	End Semester Exam (50%)			
		Review -I		Mid Review		Final Revie	W
		Th	Prac	Th	Prac	Th	Prac
Laval 1	Remember		200/		200/		200/
Level 1	Understand		2070		20%		20%
Laval 2	Apply		800/		800/		800/
Level 2	Analyse		8070		8070		80%
L	Evaluate						
Create							
Total			100%		100%		100%

Recommended Resources

Other Resources

Course Designers

1. Dr. Rituparna Chowdhury, Assistant Professor, Dept. of ECE. SRM University – AP.



Entrepreneurial Mindset

Course Code	SEC 102	Course Cotogowy	SEC		L	Т	Р	С
Course Code	SEC 105	Course Category	SEC		1	0	1	2
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	Management	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. To develop the Entrepreneurial Mindset of Students.
- 2. To provide students an overview of different aspects of starting a business.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Recall the key entrepreneurship concepts and entrepreneurial traits	1	90%	80%
Outcome 2	Identify entrepreneurial opportunities	2	80%	80%
Outcome 3	Apply entrepreneurial skills to analyze different entrepreneurial ventures.	3	70%	70%
Outcome 4	Apply entrepreneurial concepts to and develop a business model canvas	3	60%	60%

	Program Learning Outcomes (PLO)														
CLOs	Engineering Knowledge	Problem Analysis	Design and Development	Analysis, Design and Research	Modern Tool and CT Usage	Society and Multicultural Skills	Environment and Sustainability	Moral, and Ethical Awareness	Individual and Teamwork Skills	Communication Skills	Project Management and Finance	Self-Directed and Life Long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3			2				2		2	2				3
Outcome 2	1	3	3	3				3			3				1
Outcome 3	2	3	3	3				3		2	3				2
Outcome 4	3	3	3	3				3		3	3				3
Average	2	3	3	3				3		2	3				2

Unit No.	Unit Name	Required Contact	CLOs	References
11.11	Totas Justian	Hours	Addressed	Used
	Introduction	2	1,3	
1.	What is Entrepreneurship			
2.	Challenges Faced by Entrepreneurs			
3.	Why not entrepreneurship			
4.	Who is an Entrepreneurs (Characteristics			
	and Myths)			
5.	Why become entrepreneurs			
6.	Entrepreneurial Traits			
7.	Significance of entrepreneurship in the			
	economy			
8.	Types of Entrepreneurial Ventures			
Unit 2	Entrepreneurial Orientation	4	1,2,4	
9.	Characteristics of successful entrepreneurs			
10	Mindset shifts: from an employee to an			
10.	entrepreneur			
11	Overcoming challenges and dealing with			
	failures			
Unit 3	Entrepreneurial Skills	4	1,2,3,4	
12.	Innovation & Creativity			
13.	Design Thinking			
14.	Strategic Thinking			
15.	Developing a Growth Mindset			
Unit 4	Technopreneurship	2	1,2	
16.	Overview of Technopreneurship			
17.	Characteristics of a Technopreneur			
18.	Technology Trends and Disruption			
19.	Real-world Technopreneurship Examples			
Unit 5	Entrepreneurial Opportunity & Ideation	4	2	
20.	Difference between idea and opportunity			
21	Opportunities in Vibrant Indian			
21.	Entrepreneurial Ecosystem			
22	Opportunity Recognition (Sources of			
22.	Opportunity)			
23.	Assessing Opportunity			
24.	Opportunities and Uncertainty			
25.	Idea Generation & Market Research			
26.	Idea Selection			
Unit 6	Business Model Canvas & Pitching	2	1,4	
27.	Why BMC			
28.	Value Proposition			
29.	Customer Discovery			
30.	Customer Relationship			
31.	Channels			
32.	Key Partners			
33.	Key Activities			
34.	Key Resources			
35.	Revenue Structure			
36.	Cost Structure			
37.	From Pitch to Hitch (Pitch Deck)			

Unit 7	Startup Financing	2	1,4	
38.	Stages of Fund Raising			
39.	Startup Valuation			
40.	Mode of Investment			
41.	Shareholder's Agreement			
42.	Financial Analysis			
	Total Contact Hours		20	

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (100%)							
		CLA-1 (30%)	CLA-2 (30%)	CLA-3 (40%)					
Level 1	Remember	100%	40%						
	Understand	100 /0	40 /0						
Level 2	Apply		60%	100%					
	Analyse		00 /0						
Level 3	Evaluate								
	Create								
	Total	100%	100%	100%					

Recommended Resources

- Larry Keeley Brian Quinn Ryan Pikkel. Ten types of innovation -the discipline of building breakthroughs, John Wiley& Sons, Inc; 2013
- 2. Eric Ries. The lean startup how constant innovation creates radically successful businesses, Penguin Books
- 3. Bruce R. Barringer, R. Duane Ireland. Entrepreneurship Successfully Launching New Ventures, Pearson; 2020
- 4. Robert D. Hasrich, Dean A. Shepherd, Michael P. Peters, Entrepreneurship, McGraw Hill, 2020
- 5. Siva Prasad N. Design Thinking : Techniques And Approaches, Ane Books, New Delhi; 2023

Other Resources

- 1. https://www.coursera.org/specializations/innovation-creativity-entrepreneurship
- 2. https://www.coursera.org/specializations/wharton-entrepreneurship

Course Designers

- 1. Mr Aftab Alam, Assistant Professor, Paari School of Business, SRM University-AP
- 2. Mr Udayan Bakshi, Associate Director, Entrepreneurship and Innovation, SRM University-AP
- 3. Prof. Bharadhwaj S, Dean, Paari School of Business, SRM University-AP

VLSI Testing and Verification

Course Code	VI S 505	Course Category	CC			L	Т	Р	С
Course Coue	VE5 505	Course Category	ce			3	0	1	4
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)					
Course Offering Department	ECE	Professional / Licensing Standards							

Course Objectives / Course Learning Rationales (CLRs)

- 1. To ensure Quality and Reliability): As VLSI circuits become more complex and denser, the likelihood of defects and errors increases. Testing and verification techniques are employed to ensure that the fabricated chips meet the desired specifications and are free from manufacturing defects. This is crucial to ensure the overall quality and reliability of the integrated circuits used in various electronic devices.
- 2. (To detect and Fix Design Errors): During the design phase of VLSI circuits, errors and bugs can be introduced inadvertently. Proper testing and verification processes help identify these design errors early in the development cycle. This allows designers to correct the mistakes before the chips are manufactured; thus, saving time and costs associated with rework.
- 3. (Functional Verification): VLSI circuits are designed to perform specific functions. This subject is focused on verifying that these functions are correctly implemented and that the chip behaves as intended under various operating conditions.
- 4. (Performance Analysis): VLSI Testing and Verification also involve assessing the performance of the integrated circuits. This includes verifying that the chips meet the required speed, power, and area constraints specified during the design phase.
- 5. (To know about the Test Methodologies and Techniques): This subject will also cover various test methodologies and techniques used to evaluate the performance and functionality of VLSI circuits. This includes design for testability (DFT), built-in self-test (BIST), automatic test pattern generation (ATPG), and scan-based testing, among others.
- 6. (Fault Models and Test Coverage): Understanding and dealing with different fault models are essential for designing effective tests to identify potential defects in VLSI circuits. This subject will cover various fault models and techniques to achieve high test coverage.
- 7. (Manufacturability and Yield Enhancement): Testing and verification are critical for assessing the manufacturability of VLSI circuits and improving yield during the chip fabrication process. A higher yield means fewer defective chips, leading to cost savings and better overall productivity.

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Have a solid understanding of testing methodologies, verification techniques, and design-for-testability principles	2	80%	70%
Outcome 2	Acquire confidence to work on real-world projects, use industry-standard tools, and simulate various testing scenarios	3	80%	70%
Outcome 3	Gain insights into the current trends and challenges in VLSI Testing and Verification, such as dealing with increased complexity, power constraints, and manufacturing defects	4	75%	65%
Outcome 4	Be able to explore career opportunities in the semiconductor industry, particularly in roles related to design verification, validation, and test engineering	4	70%	60%

Course Outcomes / Course Learning Outcomes (CLOs)

	Program Learning Outcomes (PLO)												
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	2	2	2	2	2	1	3	3	3	3	2	2	2
Outcome 2	3	2	3	2	2	1	2	2	3	3	2	3	3
Outcome 3	3	2	3	2	2	1	3	2	3	3	2	3	3
Outcome 4	3	2	2	2	2	1	3	2	3	3	3	3	2
Average	3	2	3	2	2	1	3	2	3	3	2	3	3
Unit	Description of Tonic	Required Contact	CLOs	References									
--------	---	------------------	-----------	------------	--								
No.		Hours	addressed	Used									
Unit 1	INTRODUCTION TO VLSI TESTING	7											
1.	VLSI design flow												
2.	Overview of Verification and Testing	1											
3.	Need of pre-silicon verification	'											
4.	Need of post-silicon validation and debug												
5.	VLSI Testing needs and challenges												
6.	Possible Outcome of Testing	1											
7.	Stages of IC Product		13	1 2									
8.	Types of Testing: Implicit, Explicit		1, 0	1, 2									
9.	Production Test	1											
10.	Characterization Test	1											
11.	Reliability Test	1											
12.	Test Quality Measures	1											
13.	Yield and defects												
14.	Scope of testing and verification in VLSI design process	1											
15.	Issues in test and verification of complex chips												
Unit 2	FAULT MODELING AND FAULT SIMULATION	12											
16.	Overview of Defect, Fault, Error, Failure												
17.	Random and Systematic defects												
18	Overview of Test pattern, Test Set, Test Length,	1											
10.	Fault Coverage												
19.	Importance of Fault modeling												
20.	Introduction to Fault models												
21.	Single stuck-at-fault model	1											
22.	Fanout stem and branch for Stuck-at-fault model												
23.	Multiple stuck at fault	1											
24.	Bridging faults												
25.	Bridging fault models: Wired-OR, Wired-AND, A- Dominant	2	1,3	3, 4, 7, 8									
26.	Feedback bridging faults												
27.	Fanout Stem and Branch for Bridge Fault	2											
28.	Permanent and Transient Bridge Fault												
29.	Delay fault and its detection												
30.	Delay fault models Introduction	2											
31.	Path delay fault: Falling transition, Rising transition												
32.	Transition delay fault: Slow-to-rise (STR) and slow- to-fall (STF)	1											
33.	Overview of Transistor level or Switch level fault model												
34.	Stuck-open fault	1											
35.	Stuck-short fault												
36.	Fault Simulation Overview	1											

37.	Yield and Fault Equivalence			
Unit 3	TESTABILITY MEASURES AND ANALYSIS	6		
38.	Introduction and need of testability measures]	
39.	Testability Components: Controllability and Observability	1		
40.	Overview of Testability Analysis			
41.	Topology-based Analysis		1, 3, 4	2, 7
42.	SCOAP: Combinational Controllability and Combinational Observability	2		
43.	Probability-based Analysis		1	
44.	COP: Combinational Controllability and Combinational Observability	2		
45.	High-level Analysis	1]	
Unit 4	ATPG AND DESIGN FOR TESTABILITY METHODS	14		
46.	Test pattern generation Overview: Random and Deterministic	1	-	
47.	Incomplete ATPG		_	
48.	Combinational ATPG Introduction	2		
49.	Boolean Difference Method		_	
50.	SAT	1	_	
51.	Path-sensitization Method			
52.	Single Path Sensitization	2	1.0.0	
53.	Multiple Path Sensitization		1, 2, 3	5, 6, 7, 8, 9
54.	D Algorithm	1		
55.	PODEM	1	_	
56.	FAN	1		
57.	Sequential ATPG Introduction			
58.	Scan design			
59.	Issues in Scan Design	3		
60.	Test interface and boundary scan			
61.	Iddq testing		_	
62.	Delay fault testing	2		
63.	Built-in Self-Test			
Unit 5	VLSI DESIGN VERIFICATION	6		
64.	Design verification techniques: Introduction	1]	
65.	Techniques based on simulation approach			
66.	Techniques based on analytical approach	1	3, 4	7, 8, 10
67.	Techniques based on formal approach	1]	
68.	Functional verification		1	
69.	Timing verification	3		
70.	Formal verification			
	Total Contact	Hours: 45		

Learning Assessment

Ploom'o	Loval of Cognitiva	Contin	uous Learnin	End Semester Exam		
Bloom's Level of Cognitive		CLA-1	Mid-1	CLA-2	CLA-3	(40%)
	IdSK	(15%)	(15%)	(10%)	(20%)	
Lovol 1	Remember	65%	50%	45%	60%	50%
Leveli	Understand					
Lovel 2	Apply	35%	50%	55%	40%	50%
Level 2	Analyse					
Lovel 2	Evaluate					
Level 3	Create					
	Total	100%	100%	100%	100%	100%

Recommended Resources

- 1. L.T. Wang, C.W. Wu, and X. Wen, "VLSI Test Principles and Architectures", Morgan Kaufmann, 2006
- 2. M.L. Bushnell and V.D. Agrawal, "Essentials of electronic testing," Kluwer Academic Publishers, 2000
- George W. Zobrist, VLSI Fault Modeling and Testing Techniques (VLSI Design Automation Series), Praeger Publishers Inc, 1993
- 4. RL Wadsack, "Fault modeling and logic simulation of CMOS and MOS integrated circuits" Bell System
- 5. Technology, 1978
- 6. Hideo Fujiwara, Logic testing and design for testability, MIT Press, 1985
- 7. M. Abramovici, M. A. Breuer and A.D. Friedman, "Digital systems testing and testable design," IEEE Press, 1994
- 8. P. K. Lala, "Digital Circuits Testing and Testability", Academic Press
- 9. Stephan Eggersgluss and Rolf Drechsler, High Quality Test Pattern Generation and Boolean Satisfiability, Springer, 2012

10.

- 11. P.H. Bardell, W.H. McAnney, and J. Savior, "Built-in Test for VLSI: Pseudorandom Techniques," Wiely Interscience, 1987
- 12. Khosrow Golshan, Physical Design Essentials: An ASIC Design Implementation Perspective, Springer, 2007

Other Resources

Course Designers

 Dr. Swagata Samanta, Assistant Professor, Department of Electronics & Communication Engineering, SRM University – AP



Semiconductor Device Modelling

Course Code	VI S 506	Course Cotogowy	00			L	Т	Р	С
Course Code	VLS 500	Course Category	tt		3	0	1	4	
Pre-Requisite Course(s)	Solid State Device Physics	Co-Requisite Course(s)		Progressive Course(s)					
Course Offering Department	ECE	Professional / Licensing Standards							

Course Objectives / Course Learning Rationales (CLRs)

- 1. Learn the basics of current flow though solid-state semiconductor devices.
- 2. Understand some elementary concepts of quantum- and statistical-mechanics.
- 3. Gain knowledge of electrostatics of P-N junction diodes.
- 4. Learn the design of Bipolar transistors.
- 5. Understand the design of MOSFETs
- 6. Apply theoretical knowledge of performance of BJTs and MOSFETs using ABACUS simulation tool.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Identify current flow though semiconductor devices	2	70%	65%
Outcome 2	Identify concepts of quantum- and statistical-mechanics	2	70%	65%
Outcome 3	Discuss electrostatics of P-N junction diodes	3	70%	65%
Outcome 5	Discuss BJT and MOSFET design	3	70%	65%
Outcome 6	Illustrate the applications of MOSFETs design	3	70%	65%

	Program Learning Outcome										mes (PLO)					
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3			
Outcome 1	1	1	2	2	3	2	2	2	3	2	2	1	2			
Outcome 2	1	2	2	2	1	2	2	3	3	3	2	1	2			
Outcome 3	1	2	2	2	1	2	2	3	2	3	2	1	2			
Outcome 4	1	2	2	2	3	3	3	3	3	3	3	1	2			
Outcome 5	2	2	3									2	3			
Outcome 6	2	2	2									2	2			
Average	2	1	2	2	2	2	2	3	3	3	2	2	2			

Unit No	Unit Name	Required Contact	CLOs	References
Unit NO.	Unit Name	Hours	Addressed	Used
IInit I	Basic Semiconductor Properties & Elements of	0		
Unit I	Quantum Mechanics	,		
1	General Material Properties	2	1	1,3
2	Crystal Structure, The Unit Cell Concept	1	1	1,3
3	Simple 3-D Unit Cells	1	2	1,3
4	Bravais Lattices and Crystal Systems	1	3	1,3
5	Specific Semiconductor Lattices	1	2	1,3
6	Miller Indices, Example Use of Miller Indices	1	2	1,3
7	The Quantum Concept	1	2	1,3
8	Basic Formalism, Simple Problem Solutions	1	2	1,3
Unit II	Energy Band Theory & Equilibrium Carrier Statistics	9		
0	Preliminary Considerations, Approximate One-Dimensional	2	1	1,4
9	Analysis	2	1	
10	Extrapolation of Concepts to Three Dimensions	2	1	1,4
11	Density of States, Fermi Function	1	2	1,4
12	Equilibrium Distribution of Carriers	1	3	1,4
13	The Energy Band Diagram, Donors	1	2	1,4
14	Acceptors, Band Gap Centers	1	2	1,4
	Equilibrium Concentration Relationships, Concentration	1	2	1,4
15	and E_F Calculations.	1	2	
	Recombination-Generation Processes & Carrier	0		
Unit III	Transport	9		
16	Introduction	1	2	2,3
17	Recombination-Generation Statistics	2	2	2,3
18	Surface Recombination-Generation	2	2	2,3
.19	Supplemental R-G Information	1	2	2,3
20	Drift	1	2	2,3
21	Diffusion	1	2	2,3
22	Equations of State	1	2	2,3
	Electrostatics of P-N Junction Diodes & Introduction to	0		
Unit IV	Bipolar Transistors	9		
23	P-N Diode I-V Characteristics	1	3	2,4
24	Non-ideal Effects	1	3	2,4
25	AC Response	1	3	2,4
26	Large Signal Response	1	4	2,4
27	Schottky Diode I	1	4	2,4
28	Schottky Diode II	1	3	2,4
29	BJT Design I	1	4,5,6	2,4
30	BJT Design II	1	4,5,6	2,4
31	Heterojunction Bipolar Transistors	1	4,5,6	2,4
Unit V	MOS	9	,,,	,
32.	MOS Electrostatics	2	4	2.4
33.	MOSCAP Frequency Response	1	4	2,4
34.	MOSFET I-V Characteristics	2	4	2.4
35.	Nonideal Effects in MOSFET	2	4	2.4
36.	Modern MOSFET]	3	2.4
37	Reliability of MOSFET	1	3	2.4
	Total Contact Hours	-	45	_,.

Course Unitization Lab Plan - Tutorials

Session No.	Description of Experiments	Required Contact Hours	CLOs Addressed	References Used
1	Interactive visualization of different Bravais lattices, and crystal planes, and materials (diamond, Si, InAs, GaAs, graphene, buckyball).	2	2	4,5
2	Study of Band Models / Band Structure	2	3	4,5
3	Carrier Distributions: demonstrates electron and hole density distributions based on the Fermi-Dirac and Maxwell Boltzmann equations	2	3,5,6	4
4	Understand the basic concepts of DRIFT and DIFFUSION of carriers inside bulk semiconductors	2	3,5,6	4
5	Simulate semiconductor process modeling	2	3,5,6	4
6	Basic concept of PN Junction devices	2	3	4,5
7	Study of Solar Cells	2	3	5
8	Simulate npn and pnp Bipolar Junction Transistors (BJTs)	2	4	4,5
9	Analysis of MOS Capacitors	2	4	4
10	Implement MOSFET / Many-Acronym-Device-FET (mad-FETs)	4	4	4,5
	Total Contact Hours		22	

Learning Assessment

		С	ontinuous	Learning A	ssessments ((50%)	End Seme	ster Exam	
Bloom's L	evel of Cognitive		Theory	(30%)		Draatical	(50%)		
Task		CLA-1 (5%)	Mid-1 (10%)	CLA-2 (5%)	Mid-2 (10%)	(20%)	Th	Prac	
T = 11	Remember	60%	409/	60%	400/	5004	209/	409/	
Level I	Understand	0070	-070	0070	4070	3070	5070	4070	
Laval 2	Apply	409/	60%	409/	600/	5004	709/	60%	
Level 2	Analyse	4070	0070	4070	0070	5070	7070	0070	
Lavel 3	Evaluate								
Level 5	Create								
	Total	100%	100%	100%	100%	100%	100%	100%	

Recommended Resources

- 1. Advanced Semiconductor Fundamentals, Second Edition, by Robert F. Pierret, Pearson Education, Inc. (1983).
- 2. Semiconductor Device Fundamentals, Robert F.Perret, (1996).
- 3. Sze, S. M., & Ng, K. K. (2006). Physics of semiconductor devices. John wiley& sons.
- 4. B. G. Streetman, S. K. Banerjee, Solid State Electronic Devices, Pearson, (2016)
- 5. Arora, N. (2007). MOSFET modeling for VLSI simulation: theory and practice. World Scientific.

Other Resources

Course Designers

1. Dr. M. Durga Prakash, Asst. Professor. Dept. of ECE. SRM University - AP.



Advanced HDL based FPGA Design

Course Code	VI S 507	Course Cotogory	CC	L	Т	Р	С	
Course Code	VLS 507	Course Category	CC .	3	0	1	4	
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. To study and understand the basic principles and concepts of electronic components, devices, and circuitry, specifically related to semiconducting P-N junction.
- 2. To understand and analyze the characteristics of P-N junction diodes and their applications in designing various electronic devices and circuits
- 3. To understand, analyze, and design the Bipolar-Junction (BJT) and Field-Effect transistors (FET) based electronic circuits followed by advanced Operational amplifier (Op-Amp) based circuits.
- 4. To apply the knowledge gained in the course to real-world applications and work on practical projects to reinforce theoretical concepts.

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Define and understand the basic principles of electronic components related to semiconducting PN junction and other diodes.	2	85%	80%
Outcome 2	Understand, analyze and design the BJT & FET based electronic circuits	3	80%	75%
Outcome 3	Understand the properties of operational amplifiers, and their applications in designing and analyzing the various circuit operations (summing, integration, differentiation, filtering, etc).	3	80%	75%
Outcome 4	Apply the knowledge gained in the course to real-world applications and work on practical projects	4	75%	70%

Course Outcomes / Course Learning Outcomes (CLOs)

					Progr	am Leai	rning Ou	itcomes ((PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	2	1	3	2				1	2	3	2	2	2
Outcome 2	2	2	3	2				2	2	3	2	3	3
Outcome 3	3	2	3	2				2	2	3	2	3	3
Outcome 4	2	2	2	2				3	3	3	3	3	3
Average	2	2	3	2				2	2	3	2	3	3

Unit	Unit Name	Required	CLOs	References
No.		Contact	Addressed	
		Hours		
Unit 1	Introduction to VHDL	9		
	Introduction to HDL- History of VHDL, Pro's and Con's of VHDL	2	1	1,2
	VHDL Flow elements- Entity, Architecture, configuration package,	r	1	1,2
	library only definition	2	1	
	Data types, operators, operations	1	1	1, 2
	Signal, constant and variable	2	1	1, 2
	VHDL Modeling- Data flow, Behavioral, Structural.	2	1	1, 2
Unit 2	VHDL Programming	11		
	Concurrent constructs (when, with)	2	2,4	1,2
	Sequential Constructs (process, if, case, loop, assert, wait)	2	2,4	1,2,3
	VHDL program to implement Flip Flop, Counter, Shift register	2	2,4	1,2,3
	Multiplexer, Demultiplexer, Encoder, Decoder	2	2,4	1,2,3
	Moore, Mealy machines	1	2,4	1,2,3
	Test bench and its applications	2	2,4	1,2,3
Unit 3	System Verilog Design Verification	8	2,4	1,2,5
	The concept of Device under test (DUT)	2	2,4	1,2,5
	Complexity of verification, lexical elements of system Verilog (SV)	2	2,4	1,2,5
	Layered testbench and SV verification environment	2	2,4	1,2,5
	Basics of SV testbench, concurrency in system Verilog, object	2	2.4	1,2,5
	oriented programming, encapsulation and randomization		2,4	
Unit 4	Universal Verification Methodology (UVM)	9		
	UVM history, terminology, overview. UVM test phases, UVM test	2	2.4	1,2,5
	class		3,4	
	SV packages, TLM connections, Agents - stimulus functionality	2	3,4	1,2,5
	Agents - analysis functionality, UVM macros, UVM reporting,	1	3,4	1,2,5
	UVM subset			
	Environment components, prediction languages, uvm_config_db	2	3,4	1,2,5
	Ending a UVM test, phase ready to end	2	3,4	1,2,5
Unit 5	Overview of FPGA Architectures and Technologies	8		
	FPGA Architectural options, coarse vs fine grained, vendor specific	2	1 4	1,2,5
	issues (emphasis on Xilinx FPGA)		1,4	
	Antifuse, SRAM and EPROM based FPGAs, FPGA logic cells,	2	14	125
	interconnection network and I/O Pad		1,4	1,2,3
	System Design Examples using Xillinx FPGAs - Traffic light	2	14	125
	Controller		1,7	1,2,5
	Real Time Clock Interfacing using FPGA: VGA, Keyboard, LCD	2	1,4	1,2,5
	Total		45	

Course Unitization Plan (Lab)

Exp No.	Experiment Name	Required Contact Hours	CLOs Addressed	References Used
1	Write Verilog code to realize all the logic gates	2	1,4	1,2
2	 Write a Verilog program for the following combinational designs a. 2 to 4 decoder b. 8 to 3 (encoder without priority & with priority) c. 8 to 1 multiplexer. d. 4 bit binary to gray converter e. Multiplexer, de-multiplexer, comparator. 	2	1,4	1,2
3	Write a VHDL and Verilog code to describe the functions of a Full Adder using three modeling styles.	2	1,4	1,2
4	Write a Verilog code to model 32 bit ALU	4	1,4	1,2
5	Develop the Verilog code for the following flip-flops, SR, D, JK and T.	2	2,4	1,2,3
6	Design a 4 bit binary, BCD counters (Synchronous reset and Asynchronous reset) and "any sequence" counters, using Verilog code.	2	2,4	1,2,3
7	Write a Verilog code to design a clock divider circuit that generates $1/2$, $1/3^{rd}$ and $1/4^{th}$ clock from a given input clock. Port the design to FPGA and validate the functionality through oscilloscope	2	2,4	1,2,3

8	Interface a DC motor to FPGA and write Verilog code to change its speed and direction	2	2,4	1,2,3
9	Interface a Stepper motor to FPGA and write Verilog code to control the Stepper motor rotation which in turn may control a Robotic Arm. External switches to be used for different controls like rotate the Stepper motor (i) +N steps if Switch no.1 of a Dip switch is closed (ii) +N/2 steps if Switch no. 2 of a Dip switch is closed (iii) –N steps if Switch no. 3 of a Dip switch is closed etc.	2	3,4	1,2,3,4
10	Interface a DAC to FPGA and write Verilog code to generate Sine wave of frequency F KHz (eg. 200 KHz) frequency. Modify the code to down sample the frequency to F/2 KHz. Display the Original and Down sampled signals by connecting them to an oscilloscope	2	1,4	1,2,5
Total Co	ntact Hours		20	

Learning Assessment

Diag	Bloom's Loval of		Continuous Learning Assessments (50%)								
Cognitive Task		CLA-1 (5%)		Mid-1 (20%)		CLA-2 (15%)		CLA-3 (10%)		Exam (50%)	
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level	Remember	500/		400/	50/	2004	150/	250/	2004	250/	150/
1	Understand	3070		4070	570	3070	1370	2370	2070	2370	1370
Level	Apply	450/		2004	150/	2.00/	2004	250/	2004	250/	2004
2	Analyse	4370		50%	1370	3070	2070	2370	2070	2370	2070
Level	Evaluate	50/		50/	50/	50/			100/	100/	50/
3	Create	570		570	570	570			1070	10%	570
Total		10	0%	100%		100%		100%		100%	

Recommended Resources

- 1. Charles H. Roth, Digital System Design Using VHDL , Jr., Thomson, (2008)2nd Ed.
- 2. Douglas L. Perry, VHDL Programming by example, 4th Edition, 2002.
- **3.** SystemVerilog for Verification: A Guide to Learning the Testbench Language Features by Chris Spear, Greg Tumbush, Springer; 3rd ed. 2012 edition.
- 4. Salemi, Ray. The UVM primer: An introduction to the universal verification methodology. Boston Light Press, 2013.
- 5. W. Wolf, "FPGA based system design", Pearson, 2004. Other Resources
- 6. Bhaskar, J., A VHDL Primer, Pearson Education/ Prentice Hall (2006)3rd Ed.
- 7. SystemVerilog Assertions and Functional Coverage: Guide to Language, Methodology and Applications, by Ashok B. Mehta, Springer; 2014 edition.
- 8. Ashenden, P., The Designer's Guide To VHDL, Elsevier (2008) 3rd Ed.
- 9. David C. Black and Jack Donovan, SystemC: From the Ground Up, Springer, (2014) 2nd Ed.
- 10. Height, Hannibal. A practical guide to adopting the universal verification methodology (UVM). Lulu. com, 2012.
- 11. Clive Maxfield, "The Design Warriors's Guide to FPGAs", Elsevier, 2004
- 12. Wayne Wolf, "FPGA Based System Design", Prentices Hall Modern Semiconductor Design Series.

Course Designers

1. Dr. M. Durga Prakash, Asst. Professor. Dept. of ECE. SRM University - AP.



Project management

Course Code	VI S 508	Course Cotogowy			L	Т	Р	С
Course Code	VLS 508	Course Category	KDIP	0	0	3	3	
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	Mechanical Engineering	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. To understand the fundamentals of production and operations management.
- 2. To learn about capacity planning, plant layout, scheduling and sequencing
- 3. To learn about operation management, work study, time study
- 4. To understand about Inventory control, supply chain management

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Define and explain the basic concepts and principles of production and operations management (POM),	1	80%	75%
Outcome 2	Develop proficiency in capacity planning, plant layout etc.	2	70%	75%
Outcome 3	Able to perform work study, time study, gantt chart	3	80%	70%
Outcome 4	Explain supply chain management functions and applicaions	2	80%	75%

					Prog	gram Lea	arning O	utcomes	(PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	5 OS4	PSO 3
Outcome 1	3	1	3	2				3		3	3	2	3
Outcome 2	3	2	3	2				3		3	3	2	3
Outcome 3	3	2	3	2				3		3	3	2	3
Outcome 4	3	3	3	2				3		3	3	3	3
Average	3	2	3	2				3		3	3	2	3

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
	UNIT-I Fundamental concepts	8	1	1
1.	Production planning and control	2	1	1
2.	New product development	1	1	1,2
	UNIT-II Plant layout	8		
3.	Capacity planning, facility planning	2	1	1
4.	Plant location and layout	2	1,2	1,2
5.	Scheduling and sequencing	2	1,2	1,2
	UNIT- III Operation management	9		
6.	СРМ	3	3	1
7.	Gantt chart	3	3	2
8.	Work study, time study	3	3	1,2
	UNIT-IV- Material management	10		
9.	ABC analysis, EOQ	3	3,4	1
10.	Supply chain management	4	3,4	1
11.	Preventive maintenence	3	3,4	2
	UNIT – V Tools	10		
12.	Six sigma, Poka yoke, BPR, ERP, Kanban, ISO 9000,	5	3,4	2
13.	JIT, TQM, FMS, Push/Pull, Kaizen, CAD CAM	5	3,4	2
Total Cc)ntact hours	45		1

Learning Assessment

Diagm's Low	al of Cognitive Tesle	Contin	End Semester Exam		
DIOUIII S LEV	el ol Cognitive Task	CLA-1 10%	CLA-2 10%	50%	
Lovel 1	Remember	50%	500/	409/	200/
Level I	Understand	3070	3070	40%	3070
1	Apply	50%	500/	60%	709/
Level 2	Analyse	3070	3070	0070	/070
Lovel 2	Evaluate				
Level 5	Create				
	Total	100%	100%	100%	100%

Recommended Resources

- 1. Production and Operations Management by Bhattacharyya, Universal Press
- 2. Production and Operations Management by Panneer selvam R; Publisher: Prentice Hall of India

Other Resources

Course Designers

1. Prof. Prakash Jadhav, Professor, Department of Mechanical Engineering, SRM university AP.



Thesis I

Course Code	VI S 500	Course Cotogowy			L	Т	Р	С
Course Code	VLS 509	Course Category	KDIP	0	0	14	14	
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	Electronics and Communication Engineering	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. Survey the existing research works/literature and analyze them.
- 2. Demonstrate the skills acquired to solve a technical problem.
- 3. To have a systematic approach to solve the given problem.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Review and analyze the existing research work systematically.	3	80%	70%
Outcome 2	Attain strong technical, and domain knowledge in the field of project.	3	80%	70%
Outcome 3	Formulate the complex problem and have a systematic approach for the solution.	2	80%	70%
Outcome 4	Conduct research project	2	80%	70%
Outcome 5	Communicate the technical problems with peers and mentors to move towards appropriate solutions.	2	75%	70%

					Progr	am Leai	rning Ou	itcomes ((PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	1 OSA	PSO 2	PSO 3
Outcome 1	3	2	2				2	2	2	1	3	3	2
Outcome 2	3	3	3			1	2	1	2	1	3	3	3
Outcome 3	2	2	3	1	1	1	2	1	2	1	3	2	3
Outcome 4	2	2	3	1	1	1	2	2	3	1	3	2	3
Outcome 5	2	2	3	1	1	1	2	3	3	1	3	2	3
Average	2	2	3	1	1	1	2	2	2	1	3	2	3

The student is expected to spend a minimum of 12 hours/week on the Project work.

Learning Assessment

Diagon's Longie & Comiting Task		Cont	tinuous Learn	End Semester Exam (50%)				
Bloom's L	Bloom's Level of Cognitive Task		Review -I		V	Final Review		
		Th	Prac	Th	Prac	Th	Prac	
Laval 1	Remember		20%		20%		20%	
Level I	Understand		2070		2070		2070	
Laval 2	Apply		800/		80%		80%	
Level 2	Analyse		8070		8070		8070	
Laval 2	Evaluate							
Level 5	Create							
Total			100%		100%		100%	

Recommended Resources

Other Resources

Course Designers

1. Dr. Durga Prakash M, Department of Electronics and Communication Engineering, SRM University - AP



Industrial Practice

Course Code	М 8 510	Course Cotogowy	DID		L	Т	Р	С
Course Code	VLS 510	Course Category	KDIP		0	0	3	3
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department		Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1				
Outcome 2				
Outcome 3				
Outcome 4				

		Program Learning Outcomes (PLO)											
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1													
Outcome 2													
Outcome 3													
Outcome 4													
Average													

Unit	Unit Name	Required	CLOs	References
No.		Contact Hours	Addressed	Used
Unit 1				
Unit 2				
Unit 3				
Unit 4				
Unit 5				

Learning Assessment

Bloom's Level of Cognitive Task		Co	End Semester			
Diooni s Le			A-1 20% Mid-1 20% CLA-2 20% CLA-3 20%		CLA-3 20%	Exam (50%)
Loval 1	Remember					
Level I	Understand					
Loval 2	Apply					
Level 2	Analyse					
Loval 3	Evaluate					
Create						
Total						

Recommended Resources

1. Enter Data

Other Resources

1. Enter Data

Course Designers

1. Enter Data



Thesis II

Course Code	УЛ С 511	Course Cotogowy			L	Т	Р	С
Course Code	VLS 511	Course Category	KDIP		0	0	15	15
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. Survey the existing research works/literature and analyse them.
- 2. Demonstrate the skills acquired to solve a technical problem.
- 3. To have systematic approach to solve the given problem.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Review and analyse the existing research work in a systematic way.	3	80%	70%
Outcome 2	Attain strong technical, domain knowledge in the field of project.	3	80%	70%
Outcome 3	Formulate the complex problem and to have systematic approach for the solution.	2	80%	70%
Outcome 4	Conduct research project	2	80%	70%
Outcome 5	Communicate the technical problems with peers and mentors to move towards appropriate solution.	2	75%	70%

					Prog	gram Lea	arning O	utcomes	(PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	2 OS4	£ OSA
Outcome 1	3	2	2				2	2	2	1	3	3	2
Outcome 2	3	3	3			1	2	1	2	1	3	3	3
Outcome 3	2	2	3	1	1	1	2	1	2	1	3	2	3
Outcome 4	2	2	3	1	1	1	2	2	3	1	3	2	3
Outcome 5	2	2	3	1	1	1	2	3	3	1	3	2	3
Average	2	2	3	1	1	1	2	2	2	1	3	2	3

The student is expected to spend at least 32 hours/week on the Project work.

Learning Assessment

Blassed's Louis of Coordition Task		Cont	tinuous Learni	End Semester Exam (50%)			
Bloom's L	Bloom's Level of Cognitive Task		Review -I		v	Final Revie	W
		Th	Prac	Th	Prac	Th	Prac
Loval 1	Remember		2094		20%		2004
Level I	Understand		20%		20%		20%
Level 2	Apply		800/		80%		80%
Level 2	Analyse		8070		8070		8070
Laval 2	Evaluate						
Level 5	Create						
Total			100%		100%		100%

Recommended Resources

Other Resources

Course Designers

1. Dr. Durga Prakash M, Department of Electronics and Communication Engineering, SRM University - AP



Embedded Programming

Course Code	VLS 533	Course Category	CC		L 3	Т 0	P	C 4
Pre-Requisite Course(s)	Microprocessors and Microcontrollers	Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	Electronics and Communication Engineering	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. Understand the basics of Embedded Systems.
- 2. Learn the ARM architecture, instruction set and its assembly programming.
- 3. Learn to develop C programs for ARM processors and interfacing the peripherals.
- 4. Understand the software architectures used in Embedded Systems.
- 5. Learn the embedded system security including the network security

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand and explain the basics of Embedded Systems.	1	80%	70%
Outcome 2	Understand the ARM Cortex M Architecture, instruction set and do ARM assembly & C programming.	2	80%	70%
Outcome 3	Understand the architecture used in Embedded Software	1	80%	70%
Outcome 4	Understand the RTOS concepts and develop RTOS applications for ARM Microcontrollers.	2	80%	70%
Outcome 5	Understand various Embedded System Attacks & its security measures.	1	80%	70%

		Program Learning Outcomes (PLO)											
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	1 OSd	2 OS4	PSO 3
Outcome 1	3	2	2	1				1		1	1	1	1
Outcome 2	3	3	3	1				1		2	2	2	2
Outcome 3	3	1	2	1				1		1	2	2	2
Outcome 4	3	1	3	1				1		2	2	2	2
Outcome 5	3	1	2	1				1		2	2	2	2
Average	3	1	2	1				1		2	2	2	2

Unit	Unit Name	Required Contact	CLOs	References
No.	Omervane	Hours	Addressed	Used
Unit 1	OVERVIEW	9		
1	Embedded System Case Studies	2	1	1,3
2	Introduction to Embedded Systems	2	1	1,3,4
3	Getting to Know the Hardware	2	1	1,3,4
4	Learn How to Communicate	1	1	1,3,4
5	Getting to Know the Processor	1	1	1,3,4
6	Study the External Peripherals	1	1	1,3,4
Unit 2	ARM REFERENCE ARCHITECTURE	9		
7	ARM Processor Architecture	1	2	1,3,4
8	ARM Software Development	1	2	1,3,4
9	ARM Instruction Sets	1	2	1,3,4
10	Getting Started with Embedded Software Development	1	2	1,3,4
10	(Tools, Packages, Platforms, etc.)	I		
11	Your First Embedded Program-Hello, ARM!	1	2	1,3,4
12	The Blinking LED Program	1	2	1,3,4
13	The Role of the Infinite Loop	1	2	1,3,4
14	Compiling, Linking, and Locating	1	2	1,3,4
15	The Build Process	1	2	1,3,4
Unit 3	SOFTWARE ARCHITECTURE	11		
18	Four types of common architectures	3	3	3
19	Peripherals (drivers)	2	3	3
20	Interrupts (ISR, IVT, pitfalls, etc.)	1	3	3,5
21	Round-Robin	2	3	3,5
22	The Shared Data Problems	2	3	3,5
23	Function-Queue-Scheduling Architecture	1	3	3
Unit 4	EMBEDDED OPERATING SYSTEM	10		
27	Real-Time Operating Systems	3	4	2,8
28	Interrupt Routines in an RTOS Environment	2	4	2,8
29	Tasks and Task States	3	4	2,8
30	Tasks and Data	2	4	2,8
Unit 5	EMBEDDED PROGRAMMING AND	6		
Unit 5	SECURITY	0		
31	Embedded Systems Attacks: Uniquely Embedded	3	5	2
51	Insecurities	5		2
32	Attackers and Assets: Common Firmware	2	5	2
52	Vulnerabilities	<u>ک</u>		2
33	Java: Concurrency, Pitfalls, and Wireless Applications	1	5	2
	Total Contact Hours		45	

Course Unitization Plan – Lab

Session	Description of Experiment	Contact hours required	CLOs Addressed	Reference Used
1.	ARM Assembly language program for doing arithmetic operation.	2	2	6,8
2.	ARM assembly language program for Memory operations	2	2	6,8
3.	ARM Assembly - Interfacing memory mapped peripherals 1. Binary Counter with LEDs 2. Real Time Clock 3. Analog to Digital converter 4. Digital to Analog Converter	4	2	6
4.	C Program for peripheral interfacing 1. GPIO 2. Real Time Clock 3. Analog to Digital Converter 4. Digital to Analog Converter	4	2	6
5.	C Program for Asynchronous and synchronous serial communication 1. UART 2. I2C/SPI	4	2	6
6.	Embedded Ethernet applications	4	2	6
7.	Controller Area Network (CAN) interface	2	2	6
8.	RTOS Task Management	2	3	8
9.	RTOS Inter Task Synchronization and Inter Task communication	4	3	8
10.	Mini Capstone Project	2	2,3	
	Total Contact Hours		30	

Learning Assessment

			Continuous Learning Assessments (50%)								ter Exam
Bloom's Level of Cognitive Task		CLA-1 (15%)		Mid-1 (15%)		CLA-2 (10%)		CLA-III (10%)		(50%)	
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Laval 1	Remember	400/		200/		409/		409/		500/	
Level I	Understand	40%		3070		40%		4070		30%	
Loval 2	Apply	60%		70%		60%		60%		50%	
Level 2	Analyse	0070		/0/0		0070		0070		5070	
Laval 2	Evaluate										
Create											
Total		100%		100%		100%		100%		100%	

<u>Learning Assessment – Lab</u>

		Conti	nuous Learning Assessments (50%)	End Semester Exam
Bloom's L	evel of Cognitive. Task	Experiments (15%)	Record / Observation Note (10%)	Viva + Model (25%)	(50%)
Level 1	Remember	30%	70%	30%	30%
Lever	Understand		7070	5070	5070
Level 2	Apply	70%	30%	70%	70%
10.012	Analyse	,,,,,	5070	10,0	1070
Level 3	Evaluate				
Levers	Create				
	Total	100%	100%	100%	100%

Recommended Resources

- 1. Barr, Michael, and Anthony Massa. Programming embedded systems: with C and GNU development tools. " O'Reilly Media, Inc.", 2006.
- 2. Simon, David E. An embedded software primer. Vol. 1. Addison-Wesley Professional, 1999.
- 3. Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, MIT Press, ISBN 978-0-262-53381-2, 2017.
- **4.** Richard Barnett, Sarah Cox, Larry O'Cull, Embedded C programming and the Atmel AVR. 2 edition. Clifton Park, N.Y. : Thomson Delmar Learning (532 p).
- 5. Wolf, Wayne (2008), Computers as components : principles of embedded computing system design. 2 edition. Amsterdam : Elsevier (507 p).
- 6. Ata Elahi, Trevor Arjeski, "ARM Assembly Language with Hardware Experiments", Springer, 2015.
- 7. A.N.Sloss et al., "ARM System Developer's Guide", Morgan Kaufmann Publishers, 2004

Other Resources

Course Designers

1. Dr Ramakrishnan M. Associate Professor, Department of Electronics and Communication Engineering, SRM University - AP



Hardware Accelerators for IoT edge computing

Course Code	VI S 525	Course Cotogowy	CE		Ι	Т	Р	С
Course Coue	VLS 555	Course Category	CE		3	0	1	4
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. To understand DNN structures, Opportunities and Challenges with custom HW Accelerators and recent developments in DNN hardware/Chip Designs from various leading companies
- 2. To understand how DNN computations are mapped to various hardware platforms and understand the tradeoffs between various architectures/platforms and being able to evaluate different DNN accelerator implementations with benchmarks and performance comparison metrics
- **3.** To get familiar with emerging techniques for processing DNNs on edge devices such as Approximate Computing for DNNs, Precision scalable architectures and emerging NVMs for DNNs.
- 4. To understand and get hands on implementing various DNN architectures on hardware like CPU, GPU, FPGA, ASIC, etc.

Expected Expected **Bloom's** At the end of the course the learner will be able to Proficiency Attainment Level Percentage Percentage Clearly understand what are DNNs, models, datasets and 70% 65% **Outcome 1** 1 architectures evaluate the key design considerations for efficient DNN processing 2 70% 65% Outcome 2 and understand tradeoffs between various hardware architectures and platforms Understand and implement emerging techniques for processing **Outcome 3** DNNs on edge devices such as Approximate Computing for DNNs, 1,2 70% 65% Precision scalable architectures and emerging NVMs for DNNs, CiM **Outcome 4** Implement various models on hardware platforms 2 70% 65%

Course Outcomes / Course Learning Outcomes (CLOs)

					Prog	gram Lea	arning O	utcomes	(PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communicatio n Skills	Life-long Learning	1 OS4	2 OS4	PSO 3
Outcome 1	3	3	3	1		2				3	3	1	2
Outcome 2	3	3	3	2	1	2		3		2	3	2	2
Outcome 3	3	3	3	2		2		3		3	3	2	2
Outcome 4	3	3	3	2	1	2		3		2	3	2	2
Average	2.4	2.4	2.4	1.4	1	1.6		3		2	2.4	1.4	1.6

Unit No	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	Introduction to Hardware accelerators, IoT Edge Computing, DNNs and Applications	8	- Hun CSSCu	
1.	Overview of ML/Deep Learning and Applications,	2	1	1,2,3
2.	Training vs Inference, IoT Embedded vs Cloud Computing	2	1	1
3.	Overview of DNN Components, DNN layers, Popular types of Deep Neural Networks-FN,CNNs, RNNs, LSTM,	2	1	1
4.	Light weight NN Models	2	1	1,2
Unit 2	DNN models	10		
6.	Popular DNN models	2	1,2	1
7.	HW-SW Co-Design	2	1,2	1
8.	CNNs and implementation	3	1,2	1
9.	DNN development resources	3	1,2	1
Unit 3	DNN key metrics, Design objectives, hardware platforms	10		
10.	Accuracy, Throughput, Latency	2	2,3,4	1
11.	Power, energy, flexibility, scalability	3	2,3,4	1
12.	Designing DNN accelerators	2	2,3,4	1
13.	Accelerating DNNs in Hardware: study and analysis of various recent platforms on CPU, GPU, FPGA, ASIC platforms	3	2,3,4	1
14.	Architectures of Google's TPU, Apple's Neural Engine, ARM's Project Trillium, etc	2	2,3,4	1
Unit 4	Review of Python & Verilog for FPGA, CAD Tools for ASIC implementations	9		
15.	Review of Python for DNNs with examples	3	2,3,4	1
16.	Review and design of DNNs with HDLs	3	2,3,4	1
17.	Review of cadence EDA based system design for DNNs	3	2,3,4	1
Unit 5	Emerging Techniques for DNN processing on edge devices	8		
18.	Precision scalable architectures	2	3	1
19.	Approximate Computing techniques	2	3	1
20.	In-memory computing architectures	2	3	1
21.	Emerging NVMs for DNN processing	2	3	1
	Total		45	

Course Unitization Plan - Lab

Exp	Experiment Name	Required Contact	CLOs	References
No.	Experiment Name	Hours	Addressed	Used
1.	Edge Detection Using Image and Google Colab	4	2,3,4	1, 2
2	Hardware Implementation of Edge detection using NVIDIA Jetson	2	2,3,4	1, 2
Ζ.	Nano			
3.	MNIST Digit Classification with a CNN	2	2,3,4	1, 2
4.	Image Classification using CNNs	2	2,3,4	1, 2
5	Hyperparameter Tuning for Image	2	2,3,4	1, 2
5.	Classification			
6.	Object Detection and Implementation with Raspberry PI	2	2,3,4	1, 2
7.	Analyses of Interface Time Through Object Detection	2	2,3,4	1, 2
8.	FPGA Implementation of CNNs for Image classification	4	2,3,4	1, 2
0	Design and Implementation of Precision Scalable architecture,	4	2,3,4	1, 2
9.	Approximation circuits for DNNs			
10.	Course project Implementation	6	2,3,4	1, 2
	Total Contact Hours		30	

Learning Assessment

Place	Bloom's Level of Cognitive Task		0	Continuou	s Learnin	g Assessm	ents (50%	ó)		End Semester		
			CLA-1 (10%)		Mid-1 (15%)		CLA-2 (10%)		(15%)	Exam (50%)		
Cognitive lask		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac	
Loval 1	Remember	80%	20%	50%	20%	20%	30%	20%	20%	20%	30%	
Level 1	Understand	80%	5070	5070	5070	2070	5070	2070	5070	2070	3070	
Loval 2	Apply	200/	70%	50%	70%	80%	70%	80%	70%	80%	700/	
Level 2	Analyse	2070	/0%			8070				0070	/0/0	
Laval 2	Evaluate											
Create												
Total		100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	

Recommended Resources

- 1. Vivienne Sze , Yu-Hsin Chen , Tien-Ju Yang, Joel S. Emer, Efficient Processing of Deep Neural Networks, Springer, 2020. https://link.springer.com/book/10.1007/978-3-031-01766-7
- 2. Deep Learning by Ian Goodfellow and Yoshua Bengio and Aaron Courville, MIT Press, https://www.deeplearningbook.org/
- 3. Neural Networks and Deep Learning, http://neuralnetworksanddeeplearning.com

Other Resources

Course Designers

1. Dr. Ramesh Vaddi, Associate Professor, Dept of ECE, SRM University - AP



Sensor Technology and MEMS

Course Code	VI S 562	Course Cotogom:	CE		L	Т	Р	С
Course Code	VLS 302	Course Calegory	CE		3	1	0	4
Pre-Requisite Course(s)	VLS 513	Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. To understand MEMS and microfabrication
- 2. To study the essential material properties.
- 3. To study various sensing and transduction technique.
- 4. To know various fabrication and machining process of MEMS
- 5. To know about the polymer and optical MEMS

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Be familiar with the important concepts applicable to MEMS and their fabrication	2	70%	65%
Outcome 2	Discuss the design, analysis and testing of MEMS required material properties	2	70%	65%
Outcome 3	Discuss the various sensing and transduction techniques	3	70%	65%
Outcome 4	Discuss various fabrication and machining process of MEMS	3	70%	65%
Outcome 5	Illustrate the applications of the polymer and optical MEMS devices	4	70%	65%

					Progr	am Lear	ning Ou	tcomes (PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	I OSA	PSO 2	PSO 3
Outcome 1	1	1	2	2	3	2	2	2	3	2	2	1	2
Outcome 2	1	2	2	2	1	2	2	3	3	3	2	1	2
Outcome 3	1	2	2	2	1	2	2	3	2	3	2	1	2
Outcome 4	1	2	2	2	3	3	3	3	3	3	3	1	2
Outcome 5	2	2	3									2	3
Average	2	1.5	2	2	2	2	2	3	3	3	2	2	2

Unit	Unit Nama	Required	CLOs	References
No.	Unit Ivanie	Contact Hours	Addressed	Used
Unit I	Introduction to Microfabrication	10		
1	Review of Photolithography	2	1	1,3
2	Thin Film Deposition, Thermal Oxidation of Silicon	2	1	1,3
2	Wet Etching, Silicon Anisotropic Etching, Plasma Etching and	2	2	1,3
3	Reactive Ion Etching	2	2	
4	Doping	1	3	1,3
5	Wafer Dicing, Wafer Bonding	1	2	1,3
6	Packaging and Integration	1	2	1,3
7	Surface Micromachining	1	2	1,3
Unit II	Electrical and Mechanical Concepts	10		
8	Conductivity of Semiconductor	1	1	1,2
9	Crystal Planes and Orientations	2	1	1,2
10	Stress and Strain	1	2	1,2
11	Flexural Beam Bending Analysis Under Simple Loading Conditions	2	3	1,2
12	Intrinsic Stress, Dynamic System	2	2	1,2
13	Resonant Frequency, and Quality Factor	2	2	1,2
Unit III	Electrostatic and Thermal Sensing and Actuation	8		
16.	Parallel-Plate Capacitor, Applications of Parallel-Plate Capacitors (Inertia Sensor, Pressure Sensor, Flow Sensor, Tactile Sensor, Parallel- Plate Actuators)	2	2	2,3
17.	Interdigitated Finger Capacitors, Applications of Comb-Drive Device (Inertia Sensors, Actuators)	2	2	2,3
18.	Thermal Sensors and Actuators, Fundamentals of Thermal Transfer, Sensors and Actuators Based on Thermal Expansion	2	2	2,3
19.	Thermocouple and Thermal resistors, Applications (Inertia Sensors, Flow sensors, Infrared sensors)	2	2	2,3
Unit IV	Piezoresistive Sensors and Piezoelectric Sensing and Actuation	9		
23.	Expression of Piezoresistivity, Piezoresistive Sensor Material (Single Crystal Silicon, Polycrystalline Silicon)	2	3	1,2
24.	Stress Analysis of Mechanical Elements, Applications of Piezoresistive Sensors (Inertia Sensor, Pressure Sensor, Flow Sensor, Tactile Sensor);	4	3	1,2
25.	Mathematical Description of Piezoelectric Effects, Properties of Piezoelectric Materials, Applications (Inertia Sensor, Acoustic, Flow Sensor, Tactile Sensor).	4	3	1,2
Unit V	Polymer MEMS, Microfluidics and Case Studies	8		
32.	Polymers in MEMS, Applications of polymers	2	4	2,3
33.	Fluid Mechanics Concepts, Microfluidic channels and valves	2	4	2,3
34.	Case studies (Capacitive accelerometer, Piezoelectric Gyroscope)	2	4	2,3
35.	Case studies (DNA amplification, Microbridge gas sensor)	2	4	2,3
	Total Contact Hours		45	

Learning Assessment

		Continuo	us Learn	End Semester Exam (50%)		
Bloom's Lave	l of Cognitive Tesk		Theor			
Dioom's Leve	for Cognitive Task	CLA-1 (5%)	Mid-1 (10%)	CLA-2 (5%)	Mid-2 (10%)	Th
L aval 1	Remember		409/	60%	409/	200/
Level I	Understand	0070	4070	0070	4070	5070
Laval 2	Apply	40%	(00/	400/	60%	70%
Level 2	Analyse	4070	0070	4070	0070	/0/0
Level 3 Evaluate Create Total						
		100%	100%	100%	100%	100%

Recommended Resources

- 1. S.M.Sze, "VLSI Technology", McGraw Hill, 2nd Edition. 2008
- 2. Chang Liu, "Foundations of MEMS" Prentice Hall, 2012
- 3. 3.S D Senturia, "MICROSYSTEM DESIGN", Kluwer Academic Publishers, 2002

Other Resources

Course Designers

1. Dr. M. Durga Prakash, Assistant Professor, Department of ECE, SRM University - AP



CAD for VLSI

Course Code	VI S 520	Course Cotogomy	CE		L	Т	Р	С
Course Coue	VLS 550	Course Category	CE		3	0	1	4
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards	IEEE, Microso	oft, Cadence, Vivac	lo			

Course Objectives / Course Learning Rationales (CLRs)

- 1. To study the various CAD tools and methodologies employed in the design of VLSI circuits.
- 2. To understand the RTL (Register-Transfer Level) design, logic synthesis, physical design, and simulation.
- 3. To learn design and testing of VLSI circuits using CAD tools.
- 4. To evaluate and enhance the performance of VLSI designs through CAD tools.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Learn industry-standard CAD tools, navigating schematic capture, layout design, and verification tools for VLSI circuits.	2	80%	70%
Outcome 2	Apply theoretical concepts into practical applications.	3	70%	60%
Outcome 3	Analyse, identify bottlenecks, optimize VLSI designs for Performance, Power, and Area (PPA) using CAD tools.	4	80%	70%
Outcome 4	Exhibit adaptability to evolving CAD technologies, ensuring they stay current with advancements in the dynamic field of VLSI design.	4	70%	60%

					Progr	am Lear	ning Ou	itcomes ((PLO)				
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	1 OS4	PSO 2	PSO 3
Outcome 1	3	1	2					2				1	2
Outcome 2	3	2	3					3			1	3	2
Outcome 3	3	3	3					2			1	3	3
Outcome 4	3	3	3					3			1	3	3
Average	3	3	3					3			1	3	3

Unit No.	Unit Name	Required Contact Hours	CLOsAddressed	References
Unit 1	Introduction to VLSI Design and CAD Tools	9		
	Understand the stages of the VLSI design process, from	1	1	1.2
	conceptualization to fabrication.	1	1	1,2
	Trace the historical development of VLSI technology and	1	1	12
	its impact on computing.	1	1	1,2
	Examine key milestones and breakthroughs that shaped the VLSI landscape.	1	1	1,2
	Analyze the pivotal role of Computer-Aided Design			
	(CAD) tools in VLSI design.	1	1,2	1,2
	Discuss how CAD tools enhance efficiency, accuracy, and	1	1.2	1.2
	productivity in VLSI workflows.	1	1,2	1,2
	Explore Electronic Design Automation (EDA) tools and	1	1.2	1.2
	their roles in the design flow.	1	1,2	1,2
	Discuss the impact of CAD tools on reducing time-to-	1	12	12
	market and overall design cost.	1		
	Introduce students to a basic CAD tool interface.	1	1,2	1,2,4,6
	Conduct introductory exercises to familiarize students with	1	1.2	1246
	basic CAD operations.	1	1,2	1,2,7,0
Unit 2	Digital Design Fundamentals	9		
	Apply Boolean algebra to simplify and manipulate logical	1	23	1.2
	expressions.	1	2,5	1,2
	Design and analyze combinational circuits using logic	1	2.3	1.2
	gates.	-	_,:	-,-
	Introduce sequential circuits, including flip-flops and	1	1,2,3	1,2
	latches.			
	Discuss the concept of clocking and its importance in	1	1,2,3	1,2
	Define Register Transfer Level (RTL) design and its role			
	in VI SI	1	1,2,3	1,2
	Demonstrate the translation of high-level design concepts			
	into RTL descriptions.	1	1,2,3	1,2
	Engage students in practical RTL design exercises.	1	2,3	1,2
	Implement simple digital circuits using RTL design			,
	principles.	1	2,3	1,2
	Utilize simulation tools to validate the functionality of		2.2	1.0
	RTL designs.	1	2,3	1,2
Unit 3	Schematic Capture and Simulation Tools	9		
	Introduce functional simulation using Verilog or VHDL.	1	2,3,4	1,2,3
	Create and simulate basic digital circuits to understand	1	2.2.4	1.2.2
	functional behavior.	1	2,3,4	1,2,5
	Optimize circuit designs for better performance using	1	234	123
	timing constraints	I	2,5,7	1,2,5
	Apply simulation tools to analyze and troubleshoot real-	1	234	123
	world digital circuits.	1	2,0,1	1,2,5
	Discuss the significance of simulation in identifying design	1	2,3,4	1,2,3
	tlaws.			
	introduce advanced simulation techniques such as mixed-	1	2,3	1,2,3
			2.2.4	1.2.2
	Explore co-simulation of analog and digital components.	1	2,3,4	1,2,3
	Conduct hands-on sessions for students to create and simulate circuits using schematic capture tools.	1	2,3,4	1,2,3

	Emphasize the practical application of simulation results in	1	2,3	1,2,3
Unit 4	Logic Synthesis and Ontimization Techniques	9		
	Define logic synthesis and its role in transforming RTL descriptions into gate-level netlists.	1	2,3,4	1,2,5
	Discuss strategies for optimizing designs in terms of area, power, and performance (PPA).	1	2,3,4	1,2,5
	Introduce technology mapping as a critical step in the synthesis process.	1	2,3,4	1,2,5
	Cover advanced logic synthesis techniques, including retiming and resynthesis.	1	2,3,4	1,2,5
	Explore the impact of these techniques on design quality and efficiency.	1	2,3,4	1,2,5
	Demonstrate the application of logic synthesis techniques through practical examples.	1	2,3,4	1,2,5
	Guide students in optimizing designs for specific criteria.	1	2,3,4	1,2,5
	Discuss current challenges in logic synthesis.	1	2,3,4	1,2,5
	Explore emerging trends and future directions in logic synthesis research and development.	1	2,3,4	1,2,5
Unit 5	Physical Design and Layout	9		
	Provide an overview of the physical design process, from initial floor planning to tape-out.	1	3,4,5	1,2,5
	Introduce floor planning as a critical step in physical design.	1	2,3,4	1,2,5
	Explain the global and detailed routing stages in the physical design flow.	1	2,3,4	1,2,5
	Discuss algorithms and techniques for efficient and effective routing.	1	3,4,5	1,2,5
	Cover the significance of physical verification in ensuring design correctness.	1	2,3,4	1,2,5
	Introduce Design Rule Checking (DRC) and its role in identifying layout violations.	1	2,3,4	1,2,5
	Conduct hands-on sessions for students to implement physical design principles.	1	3,4,5	1,2,5
	Guide students through the process of floorplanning, placement, and routing.	1	2,3,4	1,2,5
	Discuss advanced topics such as clock tree synthesis and power planning.	1	2,3,4	1,2,5
	Total			45

Learning Assessment

Bloom's Loy	al of Cognitivo	Continuous Lo	earning Assessi	nents (50%)		End Semester Exam		
Task		CLA-1 (10%)	Mid-1 (15%)	CLA-2 (10%)	Mid-2 (15%)	(50%)		
Lavel 1	Remember	80%	50%	20%	20%	20%		
Level I	Understand	8070	5070	2070	2070	2070		
Lavel 2	Apply	20%	50%	80%	80%	80%		
Level 2	Analyse	2070	5070	8070	8070	0070		
Lavel 3	Evaluate							
Create								
	Total	100%	100%	100%	100%	100%		

Other Resources

Course Designers

1. Dr. Pradyut Kumar Sanki, Associate Professor, Dept. of ECE, SRM University - AP



More Than Moore's Electronics

Course Code	VI S 555	Course Cotogowy	CE		L	Т	Р	С
Course Code	VLS 355	Course Category	CE		3	1	0	4
Pre-Requisite Course(s)	VLSI Technology	Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

- 1. To explore the limitations and challenges associated with traditional Moore's Law scaling and delve into alternative approaches for improving electronic devices.
- 2. To study and analyze emerging technologies that contribute to electronic advancements, such as 3D integration, heterogeneous integration, and new materials.
- 3. To gain proficiency in designing electronic systems with an emphasis on energy efficiency, thermal management, and overall system efficiency by taking into account power optimization.
- 4. Recognize the interdisciplinary nature of More than Moore's Electronics by exploring contributions from fields such as materials science, physics, and engineering.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the limitations and challenges associated with traditional Moore's Law scaling and delve into alternative approaches for improving electronic devices	3	80%	75%
Outcome 2	Understand and analyze the emerging technologies that contribute to electronic advancements, such as 3D integration, heterogeneous integration, and new materials	4	85%	80%
Outcome 3	Design electronic systems with an emphasis on energy efficiency, thermal management, and overall system efficiency	6	80%	75%
Outcome 4	Understand the interdisciplinary nature of More than Moore's Electronics and strongly motivated towards integration of materials science, physics, and engineering research into designing future 3D- IC systems.	5	85%	75%

		Program Learning Outcomes (PLO)											
CLOs	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	2	2	3	2	2	2	3	3	3	2	1	2	3
Outcome 2	3	2	3	2	1	2	2	2	3	3	2	3	3
Outcome 3	3	2	3	2	1	2	3	2	3	3	3	3	3
Outcome 4	3	2	2	2	3	2	3	2	3	3	3	3	2
Average	3	2	3	2	2	2	3	2	3	3	2	3	3

Unit No.	Unit Name	Required Contact	CLOs	References
		Hours	Addressed	Used
UNIT I	Introduction to 3D-IC technology	14		
	Introduction to Moore's Law and MOSFET Technology	2	1	1,2,3
-	Scaling Theory	2	1	1,2,3
-	Evolution of MOSFET	5	1	1,2,3
-	Requirements to go beyond Moore's Law	2	1	1,2,3
-	Transistor scaling & Research roadmap	2	1	1,2,3
-	CMOS feature directions	1	1	1,2,3
Unit II	3D-Interconnects	6		
	Classification and advantages of 3-D Integration	1	2,4	1,2,3
	Interconnects scaling theory and performance evolution,	2	2,4	1,2,3
	3D Interconnects	1	2,4	1,2,3
	On-chip device (vs) Interconnected device	1	2,4	1,2,3
	3D device (vs) Multicore device.	1	2,4	1,2,3
Unit III	3D-Bonding	16	2,4	
	Interconnect Technology & Classification of Interconnects	1	2,4	1,2,3
	Blanket and Non-Blanket bonding	2	2,4	1,2,3
	Direct bonding and Thermo-Compression bonding	3	2,4	1,2,3
	Passivated and Un-passivated bonding	2	2,4	1,2,3
	Metallic, Dielectric and Hybrid bonding	2	2,4	1,2,3
	Bond quality characterization techniques	2	2,4	1,2,3
	Grand challenges in bonding technology	1	2,4	1,2,3
	Wafer orientation strategies in 3D stacks	2	2,4	1,2,3
	Daisy Chain	1	2,4	1,2,3
UNIT IV	Through-Silicon-Via (TSV)	6		
	TSV Classification and Fabrication methods	1	3,4	1,2,3
	TSV Integration strategies	1	3,4	1,2,3
	TSV Cooling strategies	1	3,4	1,2,3
	TSV Electrical & Thermal modelling	2	3,4	1,2,3
	TSV Testing	1	3,4	1,2,3
UNIT V	Other Si Electronics	7		
	Spintronics, Spin FET	2	4	4
	Magnetic Tunnel Junction, Spin Transistors	2	4	4
	Organic Electronics, Organic Light Emitting Diodes (OLED),	2	1	4
	Organic Thin Film Transistors (OTFT)	2	4	4
	Organic Photovoltaic Cells (OPC)	1	4	4
	Total Contact Hours		49	

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (60%)				Fnd Somostor Exom
		CLA-1 (15%)	Mid-1 (15%)	CLA-2 (15%)	CLA-3 (15%)	(40%)
Level 1	Remember	- 50%	45%	30%	50%	40%
	Understand					
Level 2	Apply	40%	50%	50%	40%	50%
	Analyse					
Laval 2	Evaluate	10%	5%	20%	10%	10%
Level 5	Create					
Total		100%	100%	100%	100%	100%

Recommended Resources

Other Resources

Course Designers

1. Dr. Patta Supraja. Asst. Professor. Dept. Of ECE. SRM University – AP With reference to Dr. Shiv Govind Singh, Professor, Dept. Of EE. IIT Hyderabad.